LOW POWER FILTERING TECHNIQUES FOR WIDEBAND AND WIRELESS APPLICATIONS

A Dissertation

by

MANISHA GAMBHIR

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2009

Major Subject: Electrical Engineering

LOW POWER FILTERING TECHNIQUES FOR WIDEBAND AND WIRELESS APPLICATIONS

A Dissertation

by

MANISHA GAMBHIR

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Approved by:

Co-Chairs of Committee,	Edgar Sanchez-Sinencio
	Jose Silva-Martinez
Committee Members,	Shankar P. Bhattacharyya
	Alexander G. Parlos
Head of Department,	Costas N. Georghiades

August 2009

Major Subject: Electrical Engineering

ABSTRACT

Low Power Filtering Techniques for Wideband and Wireless Applications.

(August 2009)

Manisha Gambhir, B.E., Delhi University, India;

M.S., Texas A&M University, College Station

Co-Chairs of Advisory Committee: Dr. Edgar Sanchez-Sinencio
Dr. Jose Silva-Martinez

This dissertation presents design and implementation of continuous time analog filters for two specific applications: wideband analog systems such as disk drive channel and low-power wireless applications. Specific focus has been techniques that reduce the power requirements of the overall system either through improvement in architecture or efficiency of the analog building blocks.

The first problem that this dissertation addresses is the implementation of wideband filters with high equalization gain. An efficient architecture that realizes equalization zeros by combining available transfer functions associated with a biquadratic cell is proposed. A 330MHz, 5^{th} order Gm-C lowpass Butterworth filter with 24dB boost is designed using the proposed architecture. The prototype fabricated in standard 0.35μm CMOS process shows -41dB of IM3 for 250mV peak to peak swing with 8.6mW/pole of power dissipation. Also, an LC prototype implemented using similar architecture is discussed in brief. It is shown that, for practical range of

frequency and SNR, LC based design is more power efficient than a Gm-C one, though at the cost of much larger area.

Secondly, a complementary current mirror based building block is proposed, which pushes the limits imposed by conventional transconductors on the power-efficiency of Gm-C filters. Signal processing through complementary devices provides good linearity and Gm/Id efficiency and is shown to improve power efficiency by nearly 7 times. A current-mode 4th order Butterworth filter is designed, in 0.13μm UMC technology, using the proposed building. It provides 54.2dB IM3 and 55dB SNR in 1.3GHz bandwidth while consuming as low as 24mW of power. All CMOS filter realization occupies a relatively small area and is well suited for integration in deep submicron technologies.

Thirdly, a 20MHz, 68dB dynamic range active RC filter is presented. This filter is designed for a ten bit continuous time sigma delta ADC architecture developed specifically for fine-line CMOS technologies. Inverter based amplification and a common mode feedback for such amplifiers are discussed. The filter consumes 5mW of power and occupies an area of 0.07 mm^2.

A humble dedication to His boundless grace

ACKNOWLEDGEMENTS

This dissertation is a result of the support, goodwill and toil of many that were associated with me over the past few years. First, I would like to convey my sincere thanks to my advisors, Dr. Edgar Sanchez-Sinencio and Dr. Jose-Silva Martinez, for their support, encouragement and technical input. My committee members Dr. Shankar Bhattacharyya and Dr. Alexander Parlos, contributed with their valuable time and input.

Success of this research is also the result of collaborations both inside Analog Mixed Signal Center and with outside agencies. I would like to thank Metal Oxide Semiconductor Implementation Service (MOSIS), United Microelectronics Corp. (UMC) and Texas Instruments for the fabrication support and LSI Corp. for financial support. I would like to thank my co-researcher and dear friend Vijayakumar Dhanasekaran for being a great example and for his camaraderie. I would also like to thank Mohamed Mostafa, Chinmaya Mishra, Lei Chen and Eric Pankratz for their collaboration in the analog-digital-converter project. Also, thanks to Patil, Shail, Soumya, Chinmaya, Kulkarni, Amit, Didem and Feyza for their friendship and goodwill.

Staff members from different offices helped me sail through bumps at various times: Ms Ella Gallagher, Ms Tammy Carda and the support staff at various university offices. I would like to thank Raghavendra Kulkarni and Dr. Adyain Karsilayan for their crucial support in maintaining IT infrastructure for the research group.

A special thanks to my parents for their patient support and unconditional love. Thanks to my brother for being there for me always and my sister whose infectious smile

lights me in the cloudiest of the times. And to my dear husband, thank you for not letting me fall….ever.

TABLE OF CONTENTS

CHAPTER Page

CHAPTER Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 Motivation and Applications

Rapid advancements in IC design technologies have spurred the growth of consumer electronics segment and vice versa. A slew of devices enabled by modern technologies such as wireless and equipped with fast computing are fueling this growth. In the past decade or so, emerging trends of system miniaturization coupled with economies of scale has armed consumers with personal and portable electronic gadgets such as cell phones, music players, DVD-CD players, digital cameras and portable notebooks. Each of these devices has custom storage. This, in turn has triggered the evolution of storage solutions and technologies.

Traditionally, due to their low cost, hard disk based solutions were essential for any substantial storage need. Recently however, flash based systems have replaced hard disks for highly portable and small form factor devices such as personal MP3 players [1]. Despite the advents in flash technology, demands of enterprise storage and entertainment computing reaffirms the position of hard disk as the primary storage device in industrial and personal computers.

Also, convergence of storage and wireless technologies has given rise to interesting futuristic products. Wireless based backup solutions or Wi-drives, wireless

---

This dissertation follows the style of *IEEE Journal of Solid-State Circuits*.

camcorders are just few of the products that provide consumer with truly mobile experience in a connected world. Anticipated demand of wireless HDTV and set-top box solutions has only acted as catalyst in this growth.

A generic system diagram with a hard disk drive read/write channel and integrated wireless subsystem is shown in Fig. 1.1. A Read channel processes and digitizes the read magnetic pulses. Much of the computing is handled in the DSP core. Communication to peripherals and devices (computers, display, TV) may be handled through the wireless subsystem.

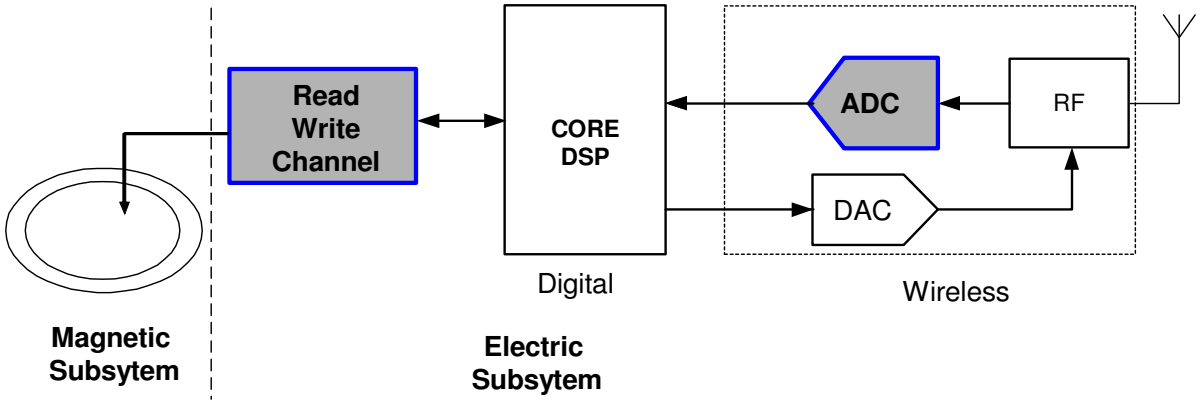


Fig. 1.1 Hard disk drive system with embedded wireless channel

Real-time processing, fast computing and entertainment applications demand faster read write operation while the speed of wireless subsystem may be dictated by prevailing standards. This dissertation concentrates on developing solutions for: A) wideband filters for disk drive channels or Multi-Gbps communication systems.

B) filters for continuous time delta sigma analog to digital converter for a wireless subsystem.

Architecture and circuit innovations are proposed with the aim of achieving the desired performance with minimum possible power consumption. Circuit techniques presented in this dissertation enable easy integration in mainstream digital CMOS technologies.

1.2 Organization of the Dissertation

The dissertation is organized around three different low power filtering solutions for storage, communication and wireless applications discussed above. Chapter II discusses architecture and implementation details of a wideband equalizing filter for disk drive applications. The initial focus of this chapter is to derive a power efficient architecture for equalizing filters. Implementation of this architecture using Gm-C based techniques is shown. Specifically, a 330MHz, 24dB equalizing gain boost filter designed for disk drive applications [2] is discussed. The achieved SNDR (Signal to Noise and Distortion Ratio) is 40dB. The prototype is realized in 0.35μm CMOS technology. Later in this chapter a 1.1 GHz 24dB boost, LC based filtering structure [3] is outlined. The chapter is concluded by drawing comparisons between Gm-C and LC based design approaches for equalizing filters.

Chapter III builds on the conclusions drawn in Chapter II and develops wideband Gm-C based filtering techniques which are nearly as efficient as LC ones. A highly efficient complementary current mirroring block is proposed and is used to implement

these filters. Such filters find their applicability in wideband communication systems or high density, high performance read channels. Specifically, the design of 1.3GHz all CMOS filter with SNDR of 55dB and power consumption of 24mW is presented. The proposed filter has been realized in 130nm digital CMOS technology [4]. The focus of this research was to fabricate a proof-of-concept design for an all CMOS, highly power-efficient filter. Hence, implementation of boost is not addressed explicitly in this solution.

Chapter IV deals with design of a filter to be utilized in a 10 bit continuous time delta sigma ADC (Analog to Digital Converter) for wireless application. Architecture of this particular ADC was developed particularly for enhanced performance in deep submicron digital CMOS technologies. Specifically, a 20MHz, 68dB dynamic range active RC filter is presented [5]. The circuit and the architecture are developed with regards to limitations imposed by 65nm digital CMOS technology with devices operating with 1.2V supply.

Finally, Chapter V outlines the conclusions from this doctorate research and future directions are discussed.

.

CHAPTER II

EQUALIZING FILTERS: DESIGN CONSIDERATIONS AND IMPLEMENTATIONS

2.1 Introduction

Fig. 2.1 shows a typical read channel for a disk drive system. It consists of a magnetic head which relays the read signals to the preamplifier. A variable gain amplifier is used to control the channel gain. In certain architectures, it is also used to introduce some pre-distortion for MRA (Magnetic Resonance Asymmetry) [6]. Lowpass filter provides necessary anti-aliasing filtering before digitization and may also embed the equalization gain. Since the dynamic range of the system is quite moderate (around 40 dB), 6-bit digitization is done using an ADC and the digital bits are passed to the digital signal processing core. This core adaptively controls the channel gain and timing loops.

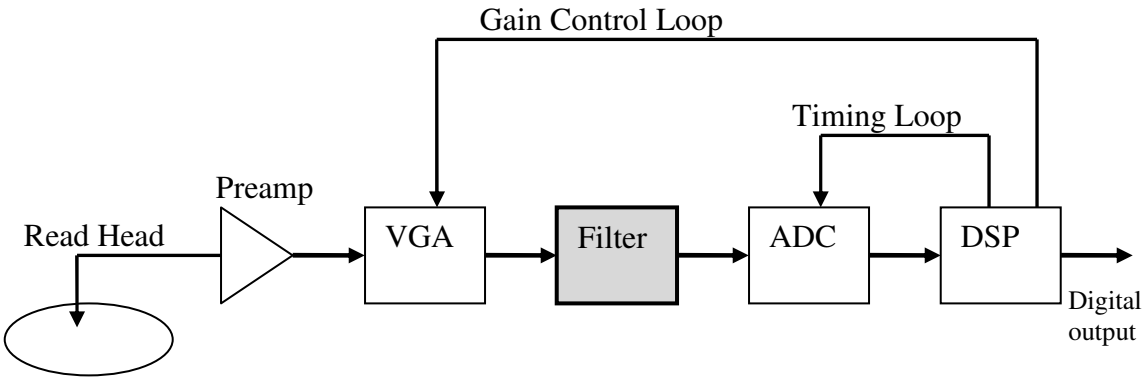


Fig. 2.1 Disk-drive read channel system

Rapid integration of storage solutions in speed driven consumer electronics and need for faster computing has resulted in increased bandwidth requirements. This implies that the transition between read pulses have become shorter giving rise to significant Inter Symbol Interference (ISI). In order to compensate for the channel losses and effectively slim the data pulses, high frequency boosting is commonly employed in such systems. Channel equalization could be carried out in the analog and/or digital domain; the partitioning of equalization gain between analog and digital domains is dictated by system integration issues, complexity of design and power trade-offs. Any magnitude equalization carried in digital domain results in boosting of the quantization noise of the ADC that follows the filter [7], thus degrading the SNR (Signal to noise Ratio). Therefore it is desirable to embed the maximum boost in the analog filter. Boost filters provide the necessary lowpass filtering before the ADC along with a programmable high frequency gain for equalization around the cut-off frequency. This chapter focuses on different aspects concerning design of this critical block.

Equalization gain for such filters (boost filters) is concentrated around the resonance frequency and typically realized by implementing multiple in-band zeros. Location of the zeros needs to be programmable in order to have controllability over the desired boost gain. Fig. 2.2 shows the pole zero constellations for the fifth order Butterworth boost filter with two equalizing zeros. The two real zeros are placed symmetrically across $j\omega$ axis such that their cumulative phase contribution is negligible.

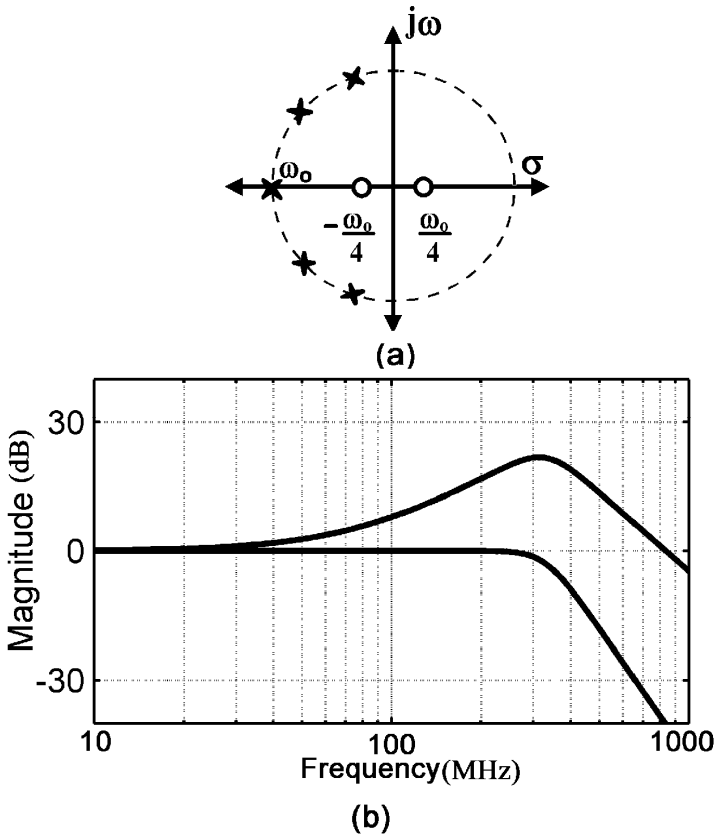


Fig. 2.2 (a) S-plane location of poles and zeros for 24dB boost setting (b) Magnitude response for 5th order Butterworth filter with 0dB and 24dB boost.

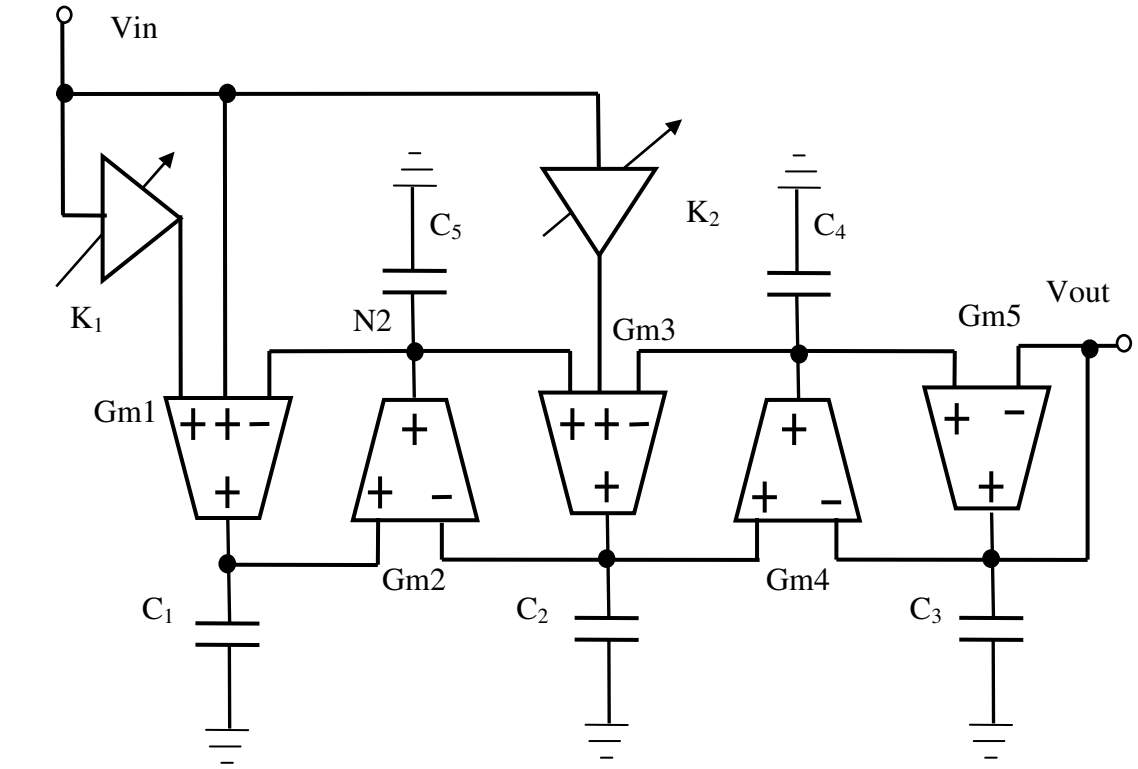
CMOS wide-band gm-C filters have been reported with bandwidth up to 550MHz [8]; but the boost filter designs reported so far have been confined to a bandwidth of 200MHz [9]-[12] and up to 14dB boost. For high speed, high density data systems, it is desirable to have maximum boost gain up to 24dB [13]. The design complexity lies with the difficulties associated with achieving high boost gains for a wide-band structure with a reasonable power budget.

This chapter explores architectural and circuit design techniques for wideband filters with high equalization gain (>20dB). Two different approaches, Gm-C and LC, are discussed. Design of a 330MHz fifth order Gm-C Butterworth filter with 24dB equalizing gain is discussed in detail. Also examined briefly is an LC equalizer realization with 1.1GHz bandwidth. Finally, the two topologies are compared for their suitability.

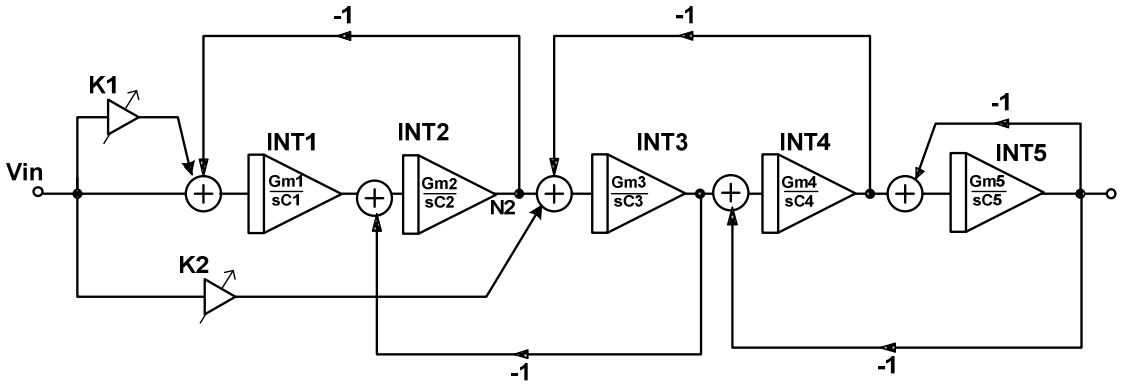
2.2 Previous Works on Filter Architectures for Disk Drives

Filter architectures reported in [9-12] implement boost gain of 12-14dB in 43MHz to 200MHz bandwidth. This section examines the drawbacks associated with these structures when used for boost gain around 24dB and a bandwidth that exceeds 300MHz.

Boost filter based on singly terminated ladder is reported in [9] for DVD (Digital Versatile Disk) applications. The fifth order representation of the reported filter is shown in Fig. 2.3. Boost is realized using a feed forward path injecting the current proportional to the input into the third integrating node. Ladder based architecture are typically less sensitive towards temperature and process variations [14]. Ladder structures consist of OTAs (Operational Transconductor Amplifiers) that are connected 'back-to-back' forming feedback loop amongst two OTAs. Any transfer-function shaping using feed-forward injection becomes complex as the feed-forward path does not always touch all the feedback loops of the ladder structure. This fact can be easily inferred from Mason's rule [15] and is mathematically illustrated in context of the architecture in Fig. 2.3.



(a)



(b)

Fig. 2.3 Singly terminated ladder based boost architecture [9]: (a) OTA representation

(b) Block diagram representation

The normalized transfer function H(s) for this architecture is given by:

$$H(s) = \frac{K_2(s^2 - 1) + K_1 - 1}{D(s)} = \frac{K_2 s^2 - 1 + K_1 - K_2}{D(s)} \quad (2.1)$$

where K_1 and K_2 are the gain of first and second feed-forward paths respectively and D(s) represents a fifth order function. The intended numerator is of the form $K_2 s^2 - 1$. The input is directly amplified and injected into the third integrating node to create the desired $K_2 s^2$ term in numerator of (2.1). However K_2 path also introduces a lowpass feed-through term $-K_2$ which needs to be cancelled through the additional feed-forward path consisting of K_1 ($K_1 = K_2$). Since unfiltered input is amplified and injected, all frequencies experience a large gain. Creating large gains at frequencies much lower than the filter's cut-off frequency and then canceling this undesired component (using an additional K_1 path) results in loss of power efficiency.

Apart from having an additional cancellation path, injecting amplified low frequency components through the feed-forward path (K_2) also has an implication that an intermediate node such as N2 (Fig. 2.3) experiences large gains at low frequencies. Fig. 2.4 shows the node swings at intermediate nodes. It is to be noted that node scaling can be done to prevent large swings at N2, but only at the expense of additional power.

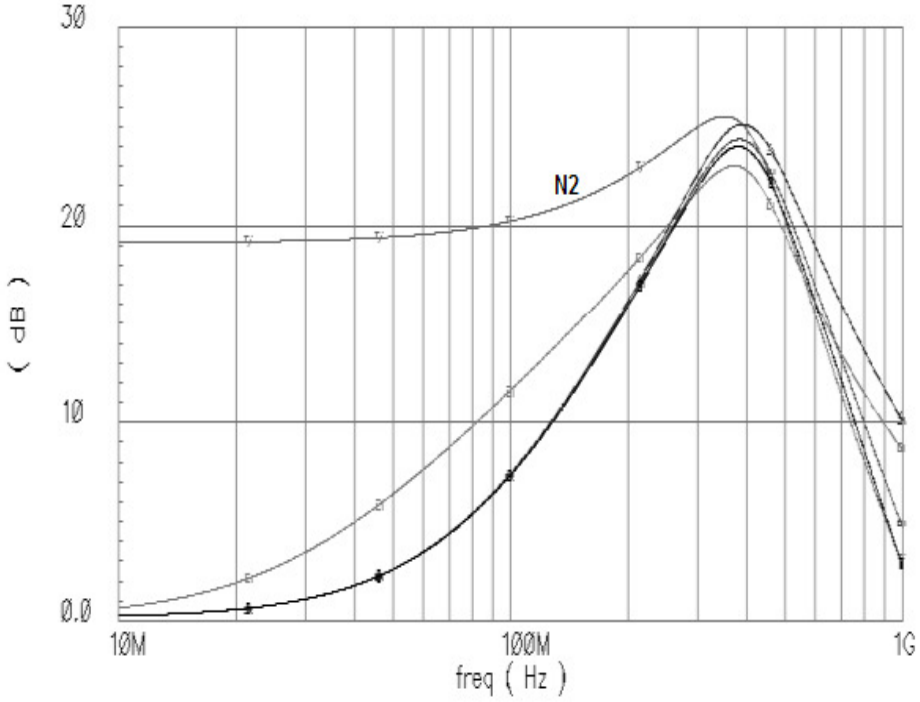


Fig. 2.4 Node swings at intermediate nodes of the boost architecture based on ladder structure of Fig. 2.3.

The third drawback of such scheme is the fact that the entire boost gain is embedded in a single gain stage consisting of K_2. This implies that for 24dB boost gain, the transconductance of the boost OTA needs to be 16 times of that of main path OTA that injects current in to the same node.

Another class of equalizing filters uses differentiation as one of the signal shaping functions. A differentiator is used in [10] to inject differentiated input signal into the lowpass node of the biquad to generate two real zeros. While there is no injection of large low frequency signal currents, keeping the differentiator parasitic poles far away

from ω_o significantly increases the power consumption [11]. Also, the entire boost gain is realized in a single stage using two zeros created by the differentiator, imposing large power requirements on its realization. The topology employed in [11] makes use of the differentiator pole as a part of a third order cell and two such cells are used to realize the complete transfer function. Note that this topology splits the boost gain amongst two cells. However, this scheme introduces one real pole for each zero realized by the differentiator, limiting the types of filter responses that may be realized. For example a fifth order Butterworth filter with two equalizing zeros cannot be realized using this scheme.

A cascade structure reported in [12] splits the boost gain between two biquads, realizing a zero each. Fig. 2.5(a) shows the biquadratic section of this architecture. This section implements a single programmable zero (through Gm15 path) apart from second order (biquadratic) filtering function. The equivalent representation for this structure using integrators is shown in Fig. 2.5(b).

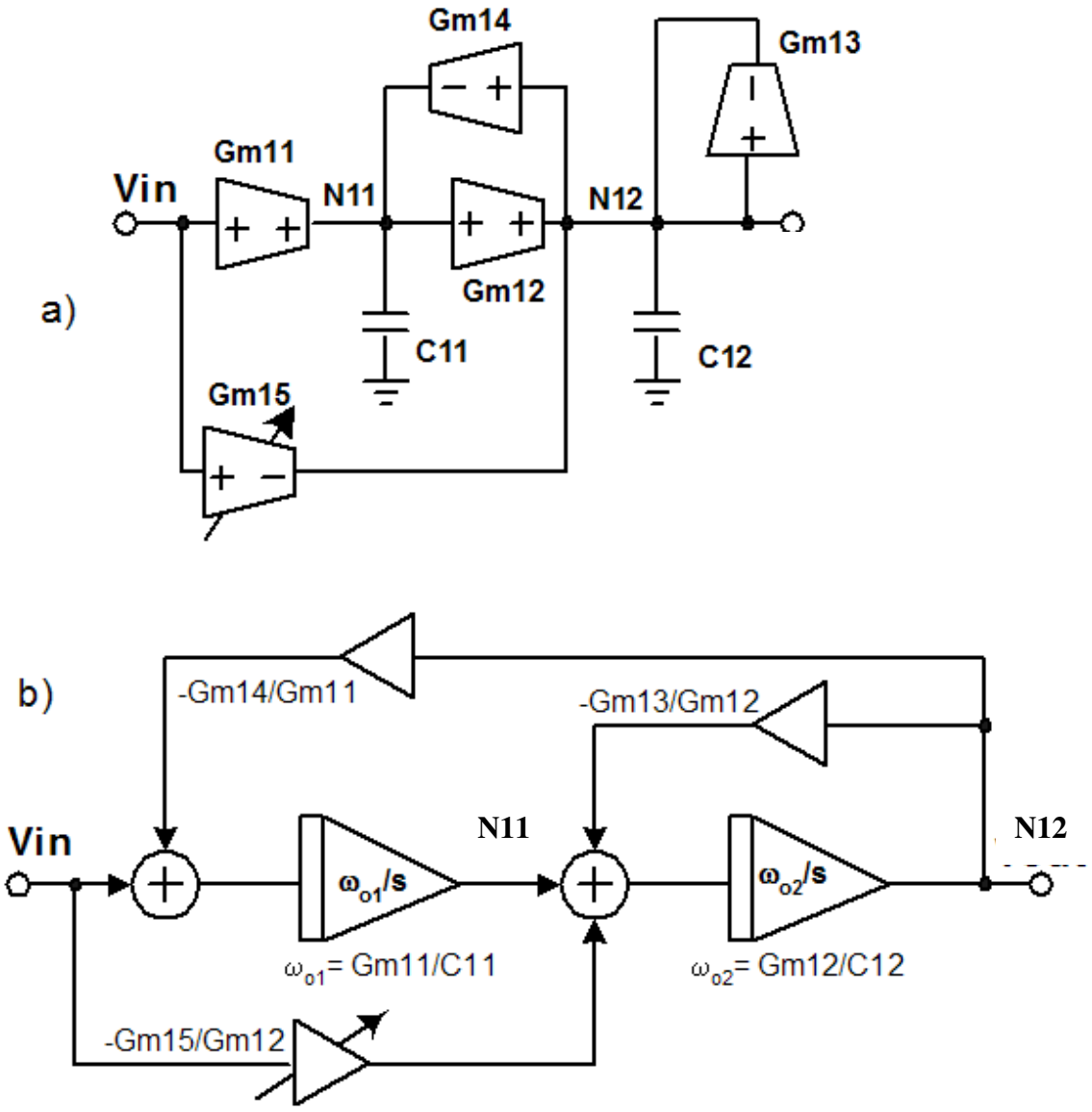


Fig. 2.5 (a) Biquad section of the filter reported in [12] (b) The equivalent integrator based representation

For a better understanding, the biquad of Fig. 2.5(a) can be represented by an '*equivalent-impedance*' model by observing the emulated impedance at node N12. The lossy OTA Gm13 is replaced by a resistor (1/Gm13) and the gyrator (Gm12, Gm14,

C11) is replaced by an equivalent inductor. Note that for the simplifying assumption that node N11 is lossless, the gyrator emulates an ideal grounded inductor. Further, the feed-forward integrating path and the programmable boost path of Fig. 2.5(a) are preserved to arrive at representation in Fig. 2.6.

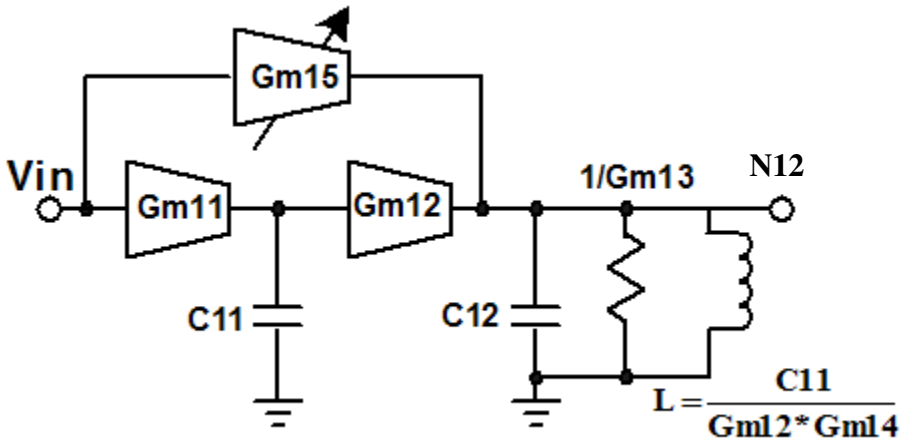


Fig. 2.6 Equivalent representation of the biquadratic section of Fig. 2.5(a)

Boost OTA Gm15 injects unfiltered signal current from the input of the biquad into the output node N12. Low frequency component of this injected current is absorbed almost entirely by the emulated inductor. This superfluous low frequency current has an indirect impact on power efficiency. Writing the current equation at low frequency or DC for node N12 (output node) under the simplifying assumption that node N11 is lossless:

$Gm15\ Vin = Gm12\ V_{N11}$ @ low frequencies (2.2)

Thus, in absence of any node scaling, the low frequency swing at node N11 increases from the nominal value of unity in accordance to the boost setting. Analytically, the low frequency component of the current generated by Gm15 is supplied by the gyrator, which makes node N11 experience gain at low frequencies. The response of different nodes for this structure (without node scaling) has been shown in Fig. 2.7. If node scaling is employed to alleviate this problem, the transconductor Gm12 has to be as large as the boost OTA, to maintain swings similar to Vin at node N11. Notice that for 24dB boost, boost OTA is about four times as large as the input OTA and there are two such biquadratic blocks in the entire filter. Further, parasitic capacitance at node N12 become prohibitively large as it is driven by two large OTAs (Gm15 and Gm12). Thus, this scaling up of transconductors adversely affects the power efficiency of this architecture especially when used for wide-band filters.

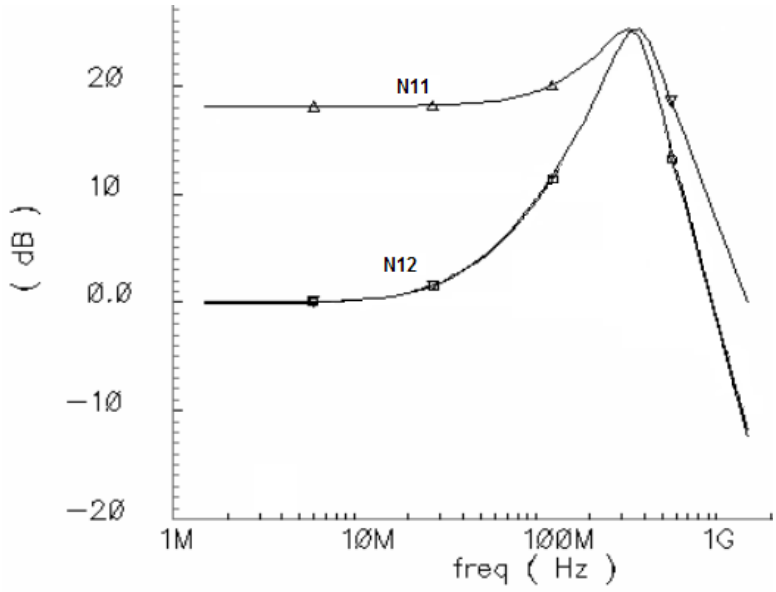


Fig. 2.7 Node swings for the biquadratic section shown in Fig. 2.5

2.3 Gm-C Based Efficient Architecture for Equalizing Filters

A power-efficient boost filter architecture is derived based on careful analysis of the demerits of previously discussed architectures. In order to be able to split the boost gain into two gain stages, cascade based architecture is preferred. The cascaded representation of the transfer function is given by:

$$H_{boost}(s) = \frac{\omega_o s\sqrt{K} + \omega_o^2}{s^2 + \frac{\omega_o}{Q1}s + \omega_o^2} * \frac{\omega_o s\sqrt{K} - \omega_o^2}{s^2 + \frac{\omega_o}{Q2}s + \omega_o^2} * \frac{\omega_o}{s + \omega_o} \tag{2.3}$$

Here, Q1 and Q2 refer to the quality factors of biquads 1 and 2 and their values are 0.618 and 1.618 respectively for the 5^{th} order Butterworth approximation. K determines the placement of zeros and its value ranges from 0 to 16 for 0 to 24dB high frequency boost. Each biquad realizes a real axis zero in addition to two poles and the gain is split between two stages in cascade.

One way to implement the zeros is to add (subtract) lowpass and bandpass voltage signals. This is done in [12] by injecting amplified current proportional to the unfiltered input voltage into the bandpass impedance node (with parallel resonator of a resistor, capacitor and emulated inductor as in Fig. 2.6). Alternately, if bandpass current is added (subtracted) from lowpass current, zeros can be directly constructed without creating the superfluous low frequency current. Thus, scaling up the transconductors, as explained in previously, is avoided. Conceptual realization (using integrators and weighted summers) of this scheme is shown in Fig. 2.8. First four integrators (INT1-4) and two summers (S1-2) can be realized using cascade of two standard biquads. $V_{LP1,2}$ and $V_{BP1,2}$ in Fig. 2.8. refer to the lowpass and bandpass nodes of biquad 1,2 respectively

and the variable gain block implements a gain of √K. Bandpass voltage is available in a standard biquad (by making the first integrator a lossy one) and it can be converted to a bandpass signal current using a variable boost transconductor. Thus, addition of bandpass and lowpass signals can be done in current mode by injecting them in the next integrating node.

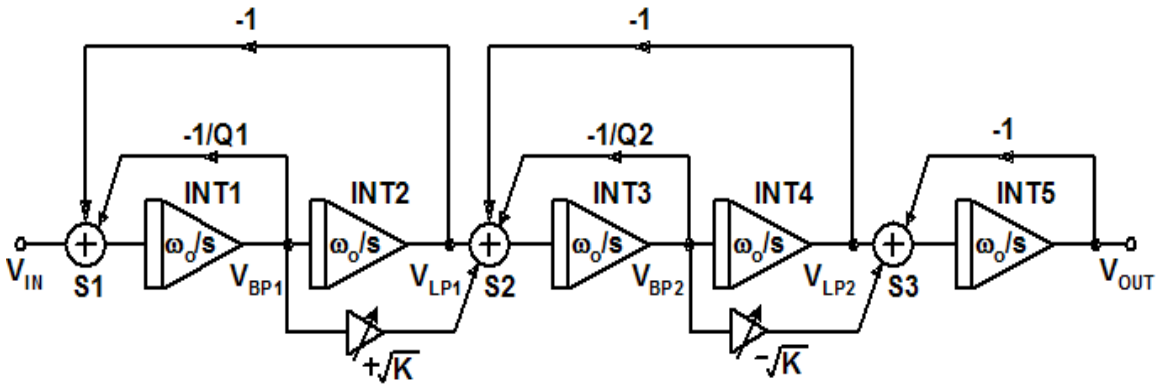


Fig. 2.8 Conceptual illustration of proposed boost filter architecture

The detailed OTA-C implementation (shown as single-ended for easy reading) of the proposed architecture is shown in Fig. 2.9 [2]. Although biquad 1 and biquad 2 generate lowpass and bandpass signals for zeros, the actual summing of the signals (in current domain) occurs at inputs of the biquad 2 and the first order section respectively.

This architecture has two salient features pertaining to power efficiency. Firstly, each stage realizes a 12dB boost gain and hence the boost path OTAs need only be $K^{1/2}$ (=4) times Gm12, Gm13. Secondly, there is no cancellation of unwanted currents at low frequencies. Since the boost OTA injects the bandpass current in the next stage, low frequency swing is always maintained around unity for all the intermediate nodes. Thus,

this architecture does not require scaling up the transconductors as against the one reported in [12].

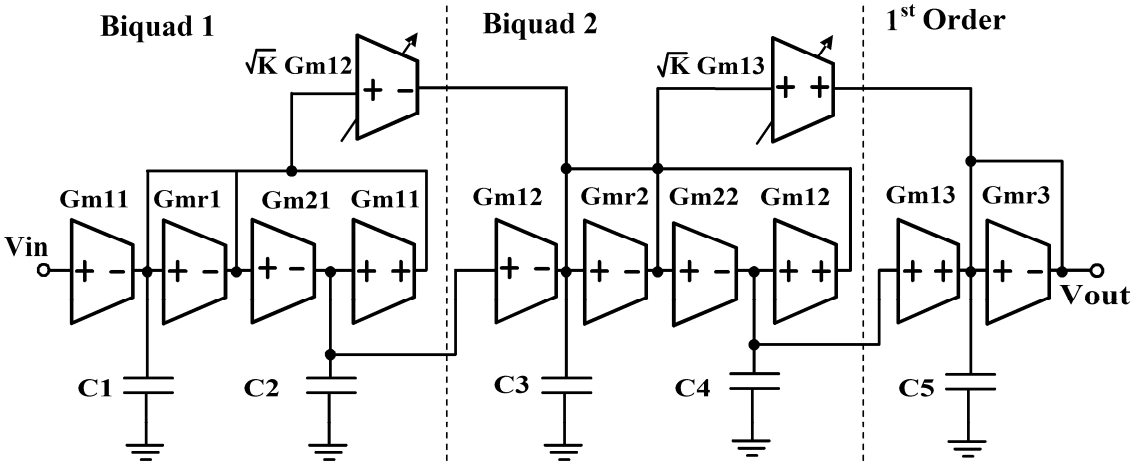


Fig. 2.9 Single ended representation of OTA-C implementation of the boost filter

Implementation of this architecture without additional summers requires the 1st order section to be the last one to provide the current summing node after biquad 2. The low Q biquad has higher input capacitance than the other biquad (its input OTA is sized to drive a larger loss-OTA). It is power efficient to keep it at the input of the filter since the low output impedance of the preceding driver will push the pole location to high frequency. Given these factors, the order of the sections is optimum if chosen as in Fig. 2.9, with biquad 1 being the low-Q section and 1st order being the last section. Also note that, for maximum boost (of 24dB) zeros are placed at $\omega o/4$. Hence, the value of K for 24dB boost is given by:

$$\frac{\omega_o}{\sqrt{K}} = 2\pi * \frac{350}{4}\text{MRad} \quad / S \qquad (2.4)$$
$$K = 16$$

Table 2.1(a) shows the relation between key component values and the filter parameters and Table 2.1(b) shows the corresponding realized values.

Table 2.1(a) Relationship between transconductance and capacitances

$Gm11/C1 = Gm21/C2 = Gm12/C3 = Gm22/C4 = Gm13/C5 = \omega_o$
$Gmr1/C1 = \omega_o /Q1 \quad Gmr2/C3 = \omega_o /Q2 \quad Gmr3 = Gm13$
$\omega_o = 2\pi*330$ M rad/s Q1 = 0.618 Q2 =1.618 Boost OTAs's transconductance = $\sqrt{K}Gm_{12}$, $\sqrt{K}Gm_{12}$ K = 16

Table 2.1(b) Transconductance and capacitor values

Stage	Gm (mS)		Capacitor pF	
Biquad1	Gm11	2.66	C1	1.15
	Gmr1	4.30	C2	0.55
	Gm21	1.27		
Biquad2	Gm21	1.27	C3	0.55
	Gmr2	0.785	C4	1.15
	Gm22	2.66		
Stage3	Gm13	1.16	C5	0.5
	Gmr3	1.16		

2.4 Circuit Implementation of Gm-C Based Equalizer

2.4.1 Core OTA

For moderate dynamic-range requirements, a single transistor operating in strong inversion and saturation region is shown to have highest transconductance (gm) and reasonable tuning range for a given W/L [16]. Hence, an OTA based on simple differential pair is desired. It can be shown (using square-law V-I relationship of MOSFET) that the third harmonic distortion component for a simple differential pair, shown in Fig. 2.10(a), is given by [17]:

$$HD_3 = \frac{V_P^2}{32 * V_{GST}^2} \tag{2.5}$$

where V_P is the peak input signal voltage and V_{GST} is the overdrive voltage (V_{GS}-V_T) fixed based on HD3 requirement (<-52dB per OTA for this case). Since the minimum V_{GST} of the input pair is fixed, power efficiency (gm/Id) cannot be improved by arbitrarily increasing W/L of transistors M1,2. OTA based on CMOS differential pair [18], as shown in Fig. 2.10(b), is used to make maximum use of available supply voltage (3.3V) for improving gm/Id under HD3 constraint.

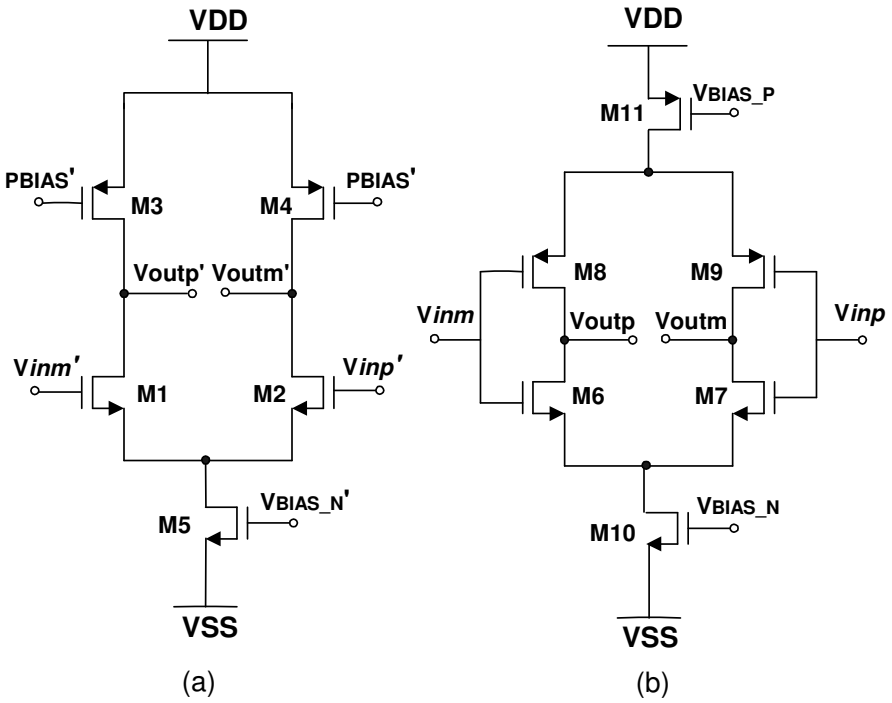


Fig. 2.10 OTA based on (a) a simple NMOS differential pair (b) CMOS differential pair

The CMOS OTA can be viewed as a NMOS OTA connected in parallel with a PMOS OTA; so as to facilitate reuse of bias current. Let m be the ratio of PMOS W/L to NMOS W/L of the CMOS OTA. Following can be written about the net transconductance GM:

$$GM = gm_N + gm_P = gm_N * (1 + \sqrt{m * \frac{Kn}{Kp}}) \quad (2.6)$$

where gm_N and gm_P represent the transconductance of NMOS and PMOS drivers respectively of the CMOS OTA. Kn and Kp are proportional to the mobility of n-channel and p-channel devices.

In order to illustrate the benefit of using CMOS OTA following expressions are formulated:

$$\frac{GM}{Id} = \frac{gm_N + gm_P}{Id} = \frac{gm_N}{Id}\left(1+\sqrt{m*\frac{Kp}{Kn}}\right) = \frac{2}{V_{GST\_N}}\left(1+\sqrt{m*\frac{Kp}{Kn}}\right) \tag{2.7}$$

$$\frac{GM}{Cin} = \frac{gm_N + gm_P}{Cgs_N + Cgs_P} = \frac{gm_N}{Cgs_N}\frac{\left(1+\sqrt{m*\frac{Kp}{Kn}}\right)}{(1+m)} \tag{2.8}$$

where Cin, Cgs_N and Cgs_P are total, NMOS driver and PMOS driver input capacitance of the CMOS OTA respectively. As evident from (2.7), by employing CMOS OTA, higher net transconductance can be realized for given bias current Id (minimum V_{GST} of the drivers is limited by distortion requirement as per (2.5)). However, addition of PMOS drivers contributes to the increased input capacitance as shown in (2.8). For the practical case of Kp<Kn; input capacitance increases by a factor of $\frac{1+m}{\left(1+\sqrt{m*\frac{Kp}{Kn}}\right)}$ for a given realized transconductance (GM).

Table 2.2 compares simple NMOS OTA (Fig. 2.10(a)) with CMOS OTA (Fig. 2.10(b)) for a given net transconductance GM. The analysis also assumes that the NMOS transistors (for both the OTAs) are sized so that V_{GST} is based on minimum value predicted by (2.5). Kn/Kp ~ 3 is used based on technology parameters.

Table 2.2 Comparison between NMOS and CMOS OTA

Parameter	NMOS OTA	CMOS OTA
$\frac{W}{L}$	$\left(1+\sqrt{\frac{m}{3}}\right)\frac{W}{L}$	NMOS =W/L, PMOS = m(W/L)
Id	$\frac{1}{2}GM * V_{GST\_N}$	$\frac{1}{2}\frac{GM * V_{GST\_N}}{1+\sqrt{\frac{m}{3}}}$
C_{INPUT}	$\left(1+\sqrt{\frac{m}{3}}\right)WLC_{OX}$	$(1+m)WLC_{OX}$
gm/Id	$\frac{2}{V_{GSTN}}$	$\frac{2}{V_{GSTN}}\left(1+\sqrt{\frac{m}{3}}\right)$
$Supply_{(MIN)}$	$V_{GST\_N5}+V_{GSN1,2}+2V_P+V_{GST\_P3,4}$	$V_{GST\_N10}+V_{GSN6,7}+2V_P+V_{GST\_P11}+V_{GSP8,9}$
Input referred noise power (v_n^2)	$\frac{4KT}{GM}(1+\frac{gm3+gm4}{GM})$	$\frac{4KT}{GM}$

Note that, for Kn/Kp = 3; $V_{GST\_P} = \sqrt{\frac{3}{m}}\,V_{GST\_N}$. For small values of m, headroom requirement of PMOS differential pair (M8,9) increases drastically (partly due to mobility degradation). On the other hand, for m greater than 3, V_{GST} of the PMOS differential pair becomes less than the minimum value mentioned above. For example, for V_{GST_N} = 200mV and Vt=500mV, choosing m=3 would result in increased headroom requirement by~700mV (as per expressions in table 2.2. As a good trade-off between headroom, power efficiency and total input capacitance, m is chosen to be 1.5. With this

value of m, gm/Id improves by 70% for additional input capacitance of 46% (relative to simple NMOS OTA) while meeting headroom and HD3 constraints.

2.4.2 Boost OTA

In order to adaptively minimize ISI across varying conditions, system typically requires that the boost gain be variable; 0dB to 24dB. This implies that the boost OTA must be widely programmable (0 to 5.1mS) and should maintain an HD3 < -52dB across the entire range. There have been various techniques proposed for widely programmable high frequency OTAs [11]-[12]. However, as the control input is varied, the input and the output capacitance offered by these OTAs changes drastically, affecting the filter's time constants. The use of such OTA as boost transconductor for wideband applications (where parasitic are a significant fraction of overall capacitance at an integration node) would not only affect the shape of the filter response but also the linearity across boost settings. Hence it is desirable to use a programmable OTA whose input and output capacitance remains invariant across boost control. OTAs with wide tuning range have been reported in [19]-[20]; but their frequency of operation is limited due to the presence of multiple nodes or the use of transistors operating in linear region. In [21], a variable transconductor that uses an additional dummy transistor pair connected to the input is employed for bandwidth programmability. The sum of the bias currents of the main input pair and the dummy pair is made constant so that the total gate capacitance ($C_{GS\text{-}total}$) remains constant. If this transconductor is used as a boost OTA and the boost gain is to be varied in fine steps, it would involve multiple of such elements. This would not

only increase the total gate capacitance (since the overlap capacitances and C_{GB} is present even in off conditions) but also add to the routing capacitance. Such increase in parasitic capacitance would impair the bandwidth of the filter, especially when it is required to drive a large transconductor in the boost path.

The structure employed in this work is based on the well-known Gilbert-cell based mixer. The proposed boost OTA is widely and continuously programmable and preserves same input and output capacitance across boost settings. Fig. 2.11 shows the schematic of the boost OTA. The voltage to current conversion is done using the main differential pair (M1,2). Pairs of common-gate control transistors (M3=M4=M5=M6) are used to steer the signal current generated in the differential pair. These control transistors are driven by differential boost control voltage (V_{CNTRL_N}-V_{CNTRL_P}) riding over the required common mode. In case of 0dB boost, differential input to the control transistors is zero. Complete cancellation of the cross-coupled currents in this case implies that no signal current is output for this setting. By varying the differential boost control voltage to the control transistor pairs (M3-6), partial cancellation of the signal current (generated by M1,2) occurs and thus the fraction of the signal current that is allowed to reach the output is controlled.

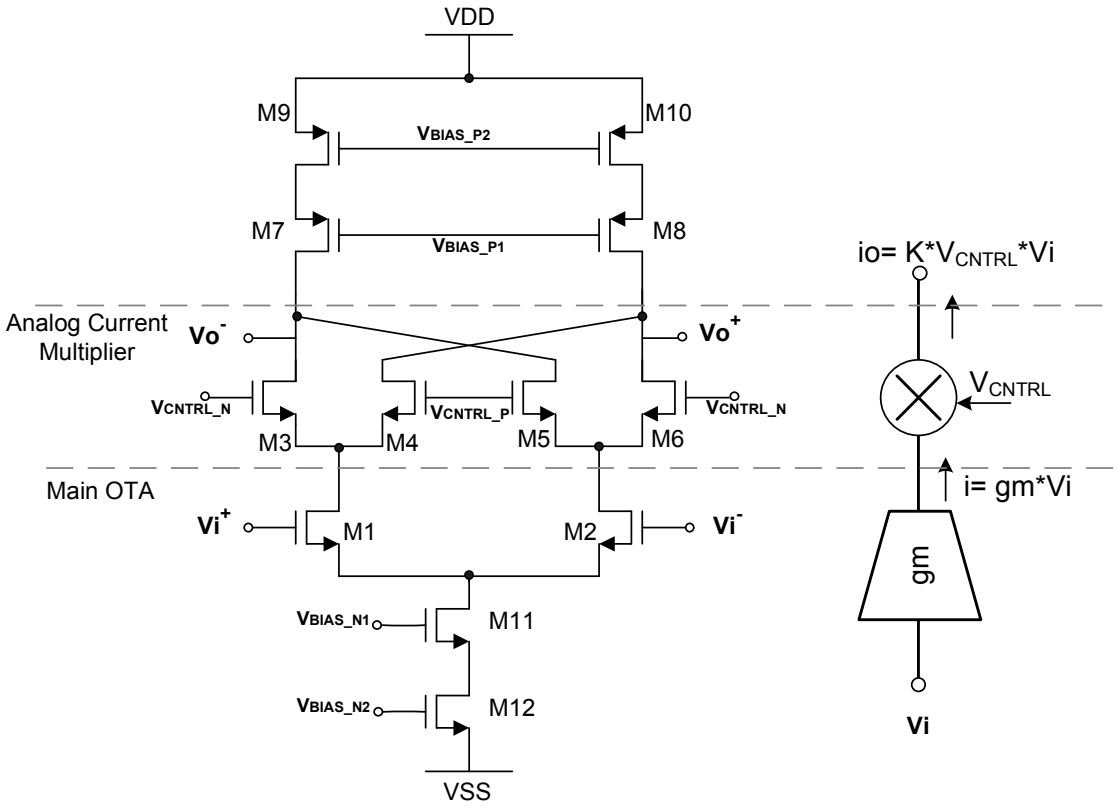


Fig. 2.11 Circuit diagram of the boost OTA

Ignoring secondary effects, the bias conditions for the driver transistors (M1,2) remain the same across boost settings. Therefore, the input capacitance does not vary across 24dB boost (12 dB per boost OTA). Since the outputs of the boost OTA are well controlled through a common mode feedback loop, the output capacitance comprising mainly of C_{db}, C_{dg} remains invariant across the boost range as well. Notice that the boost OTA does have an internal pole at the source of common-gate control transistors (M3-6). The lowest frequency of this pole occurs when large boost control voltage steers the

current of M1(2) through a single transistor; e.g. M3(6). In this case the pole location is approximately given by:

$$\omega_P \approx \frac{gm_{3,6}}{C_{gs3,6} + 2C_{sb3,6} + C_{db1,2}} \tag{2.9}$$

where $gm_{3,6}$ represents the transconductance of the transistor M3,6, $C_{gs3,6}$ and $C_{sb3,6}$ represent gate-source and source-bulk capacitance of M3,6 and $C_{db1,2}$ represents drain-bulk capacitance of the driver transistors M1.2. For a boost OTA used in the filter, this pole is located around 1.9 GHz. This additional pole in the boost path causes an error of <2% in group delay as verified through simulations of the filter's model.

2.4.3 High DC Gain, Wideband Common Mode Feedback

In order to achieve robust Q for biquads across supply voltage variations, process corners and mismatches, it is important to maintain constant operating currents for the OTAs. To maximize the available headroom for current sources under such adverse conditions, the common mode (CM) voltages must be maintained accurately. A common-mode feedback (CMFB) loop used in this design is shown in Fig. 2.12. The output CM voltage of OTA1 is sensed at the common source node of M1' and M2' by an error amplifier (EA) and the correction voltage is applied to the gate of M5. Note that Vcontrol2 (gate of next M5') is controlled by the next CMFB loop.

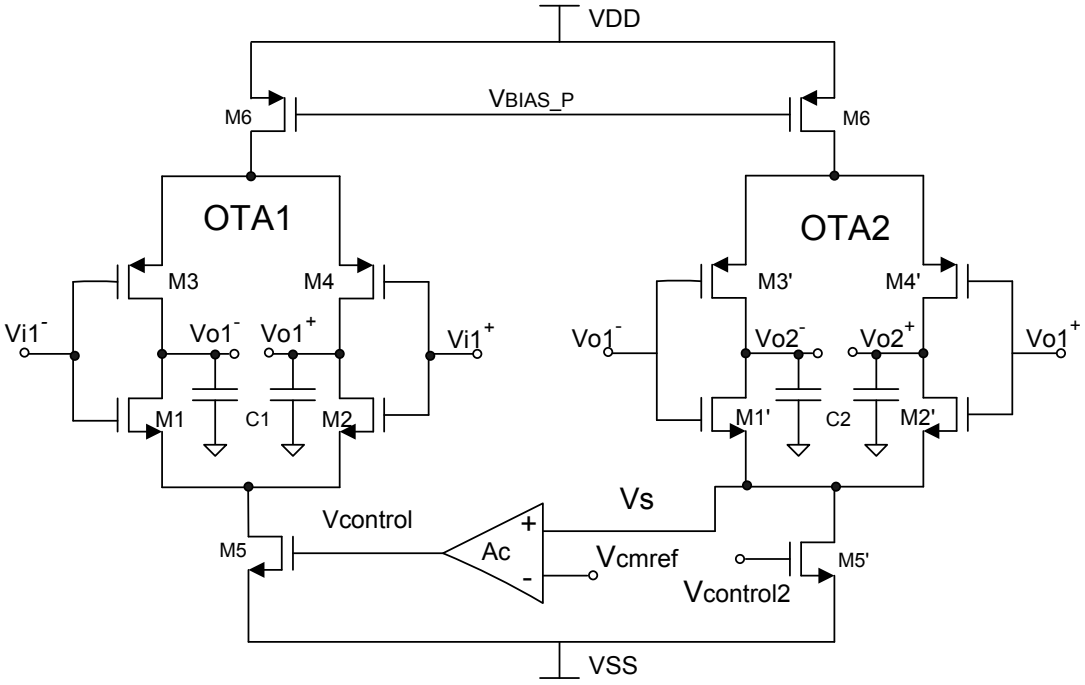


Fig. 2.12 CMFB loop involving two core OTAs and a CMFB amplifier

If ΔI is the offset current of OTA1 and $A_C(0)$ is the DC gain of the EA, the error in the output CM voltage (CM offset) of OTA1 under closed loop condition is simply given by $\Delta I/(gm_5*A_C(0))$. This can be viewed as the offset current being absorbed by the offset voltage times the DC transconductance gain of the loop ($gm_5*A_C(0)$). Thus the CM accuracy is determined by the transconductance gain and the fact that the OTA output has large CM gain is non-consequential. With conventional EA (PMOS differential pair with diode connected NMOS loads), it is observed that the CM offset voltage can be up to +/-100mV due to limited DC gain $A_C(0)$. A high gain EA is proposed in [22] to solve this problem. However, this is not widely used due to the

complexity of the circuit. A simple EA, that has large DC gain for CM accuracy yet maintains stability under wideband condition, is introduced next.

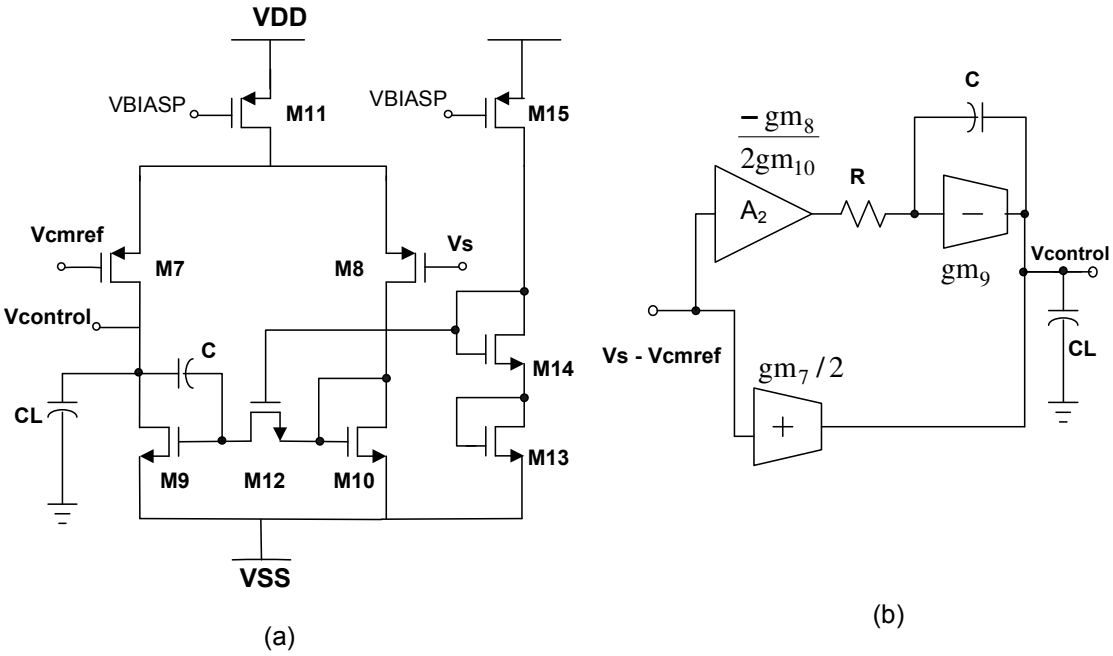


Fig.12.13 (a) Circuit diagram for the proposed CMFB error amplifier (b) Its equivalent representation

The proposed EA, shown in Fig. 2.13(a), consists of PMOS input pair (M7,8) with NMOS load (M9,10) provided with an auxiliary network consisting of a triode-MOS transistor (M12) with resistance R and a poly-capacitor C. The equivalent circuit in Fig.2.13(b) shows two parallel paths. The fast path ($1/2*gm_7$) and the slow path (A2 and gm_9) together determine the DC gain of the EA. The purpose of the network around gm_9 is to provide high output impedance at low frequencies and low output resistance ($1/gm_9$) at frequencies close to the unity gain bandwidth of the complete CMFB loop.

This characteristic manifests as a low frequency pole and a zero. If R (M12) is designed such that R >> $1/gm_{9,10}$ then the transfer function of the proposed EA is approximately given by:

$$\frac{V_{CONTROL}}{V_S'} = \frac{-gm_{7,8}R_0\left(1+s\frac{RC}{2}\right)}{1+s[RC(1+R_0gm_{9,10})+R_0C_L]+s^2RR_0CC_L} \tag{2.10}$$

where $R_O = 1/(gds_7+gds_9)$ and $C_L = Cgs_5+Cdb_9+Cdb_7$. The poles and zero of the error amplifier are located at:

$$\omega_{p\_nw} \approx \frac{1}{gm_{9,10}R_0RC} \quad , \quad \omega_{z\_nw} \approx \frac{2}{RC} \quad , \quad \omega_{p\_nd1} \approx \frac{gm_{9,10}}{C_L} \tag{2.11}$$

Thus, ω_{p_nw} is located at low frequency while ω_{z_nw} is placed at medium frequency.

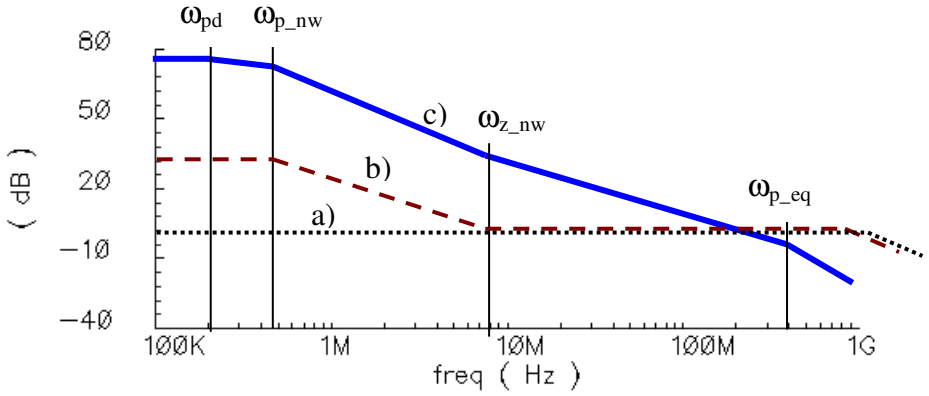


Fig. 2.14. Bode plot for (a) conventional CMFB error amplifier (b) proposed CMFB error amplifier (c) complete CMFB loop

The bode plots of the conventional and the proposed EA are shown in Figs. 2.14(a) and 2.14(b) respectively. The proposed EA displays high DC gain. However, at frequencies greater than ω_{z_nw}, it behaves like the conventional EA thus retaining similar unity gain bandwidth. In order to minimize disturbance in the relative placement of ω_{p_nw}, ω_{z_nw} and the non-dominant poles across process corners, M12 is biased using the commonly used circuit shown in Figure 2.13(a). For stability analysis, entire CMFB loop needs to be considered. In addition to EA's poles and zeros, the CMFB loop introduces one dominant pole and two non-dominant poles. Bode plot for the complete CMFB loop employing the proposed EA is shown in Fig. 2.14(c). The overall response shows a high gain CMFB loop (which results in high common mode accuracy) with stable operation (due to non dominant poles at high frequency).

2.5 Experimental Results for Gm-C Based Equalizer

The proposed 5^{th} order Butterworth boost filter has been fabricated in TSMC 0.35μm technology through MOSIS. Capacitors are fabricated using arrays of poly-poly unit cells. Common centroid techniques are used for layout of capacitor arrays and transistors. The chip micrograph is shown in Fig. 2.15. This filter occupies an area of $0.5mm^2$. A dual supply of +/-1.65V is used for all experiments.

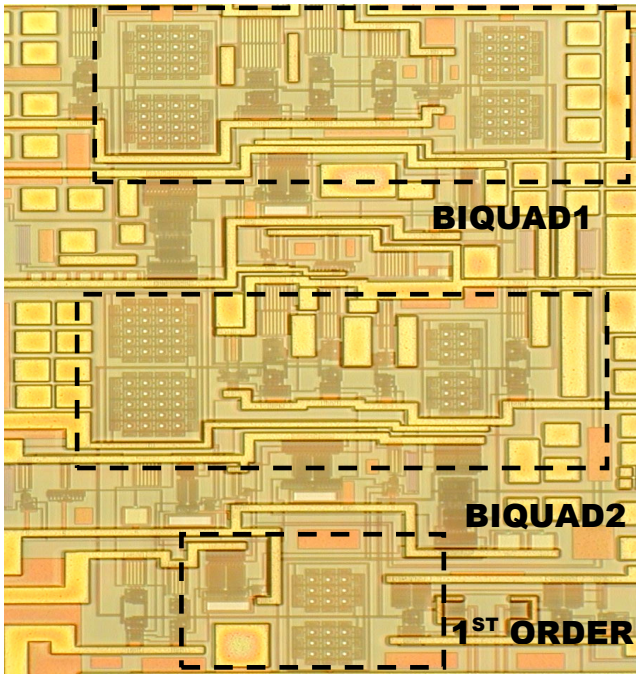


Fig. 2.15 Chip micrograph

Fig. 2.16 shows the test and measurement setup used to characterize the filter. In order to drive the pin and external capacitors, a driver buffer/OTA is included on chip following the main filter. The main filter is characterized by applying input signal through a network analyzer or a signal source. The single ended input from these instruments is converted to differential signal through a high frequency balun that is placed on-board. Another balun is placed at the output of the filter to convert the differential signal to a single ended one. This output is then characterized by network analyzer (for transfer function measurements) or spectrum analyzer (for SNDR measurements). Error in the transfer function due to additional driver/buffer, transmission balun loss is calibrated using a standalone calibration path constituting of just the replica driver and input and output terminations.

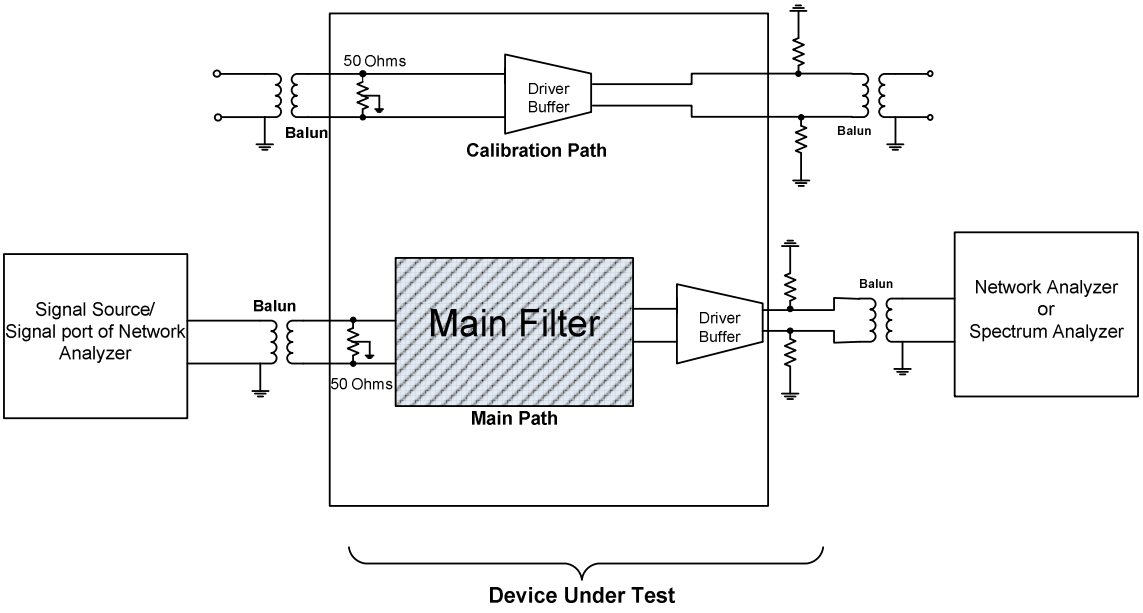


Fig. 2.16 Test setup for the measurement of filter's characteristics

Fig. 2.17 shows the filter transfer function obtained across various boost settings. The 3dB bandwidth measured with 0dB boost setting is 330MHz and the maximum achievable boost is about 24dB. Fig. 2.18 shows the group delay response of the filter; the group delay around cutoff frequency varies by 400pS (16%) between 0dB to 24dB boost. This is attributed to the finite output impedance of OTAs.

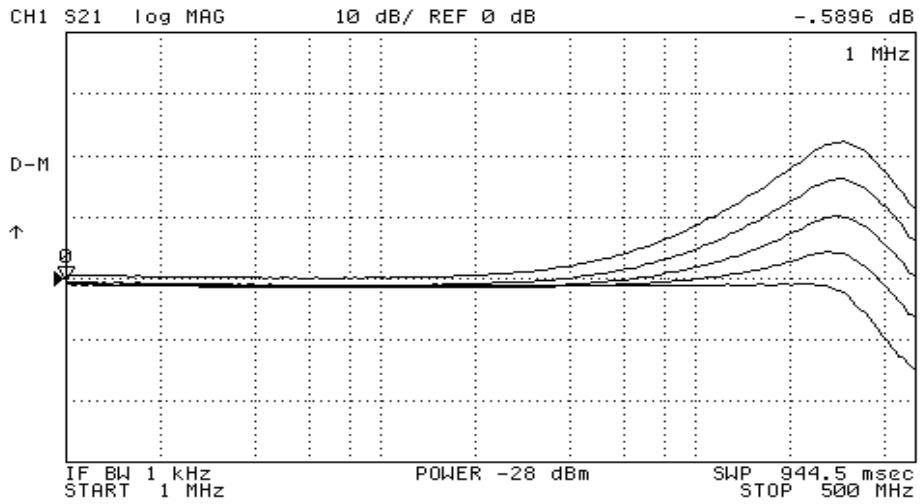


Fig. 2.17 Measured transfer function of the filter for varying boost gains

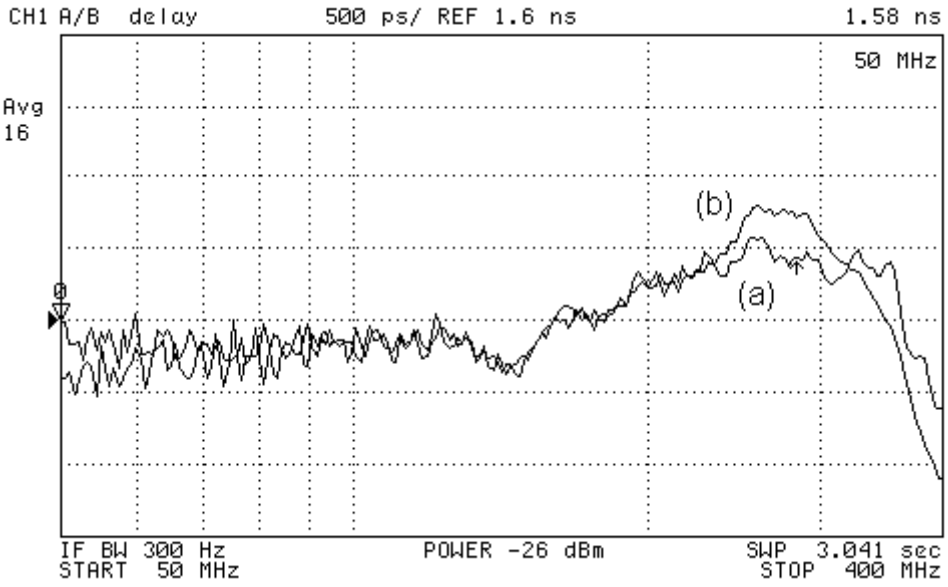


Fig. 2.18 Measured group delay for 0dB (trace a) and 24dB boost conditions (trace b)

Filter's linearity performance was measured around the highest frequency of interest using two-tone intermodulation tests. Fig. 2.19 shows the spectrum obtained

from this test: two tones are applied at 304MHz and at 307MHz with 250mV of total peak to peak swing; boost gain was set to 0dB. The measured third intermodulation distortion (IM3) is around -41 dB. For measuring IM3 performance with highest boost setting, input tones are scaled down to maintain the output power at the specified value. IM3 with 24dB boost setting is measured to be -45dB. Improvement in distortion performance with higher boost settings can be explained by the fact that in this case voltage swing at the initial filter stages is smaller. However, the output swing is maintained at the rated value (there is a significant gain around the frequency of the tones).

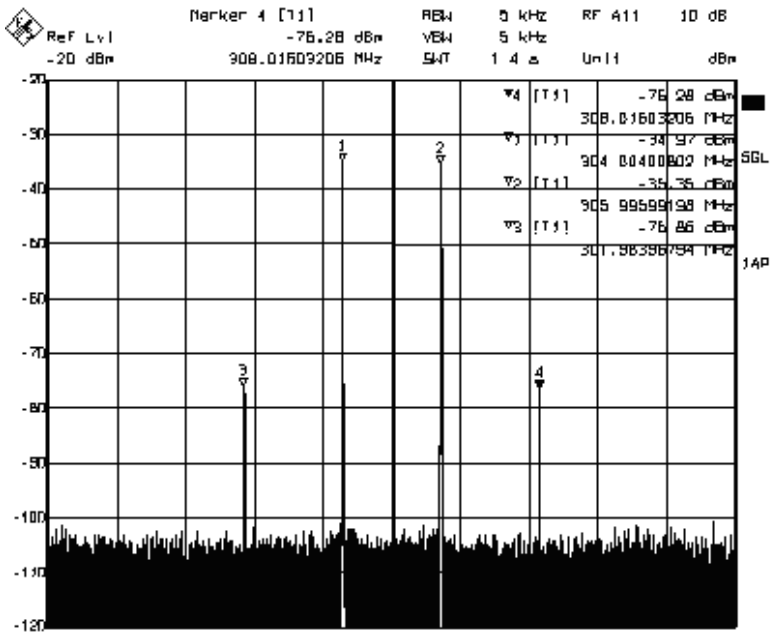


Fig. 2.19 Intermodulation test for the boost filter with tones at: f_{O1}=304MHz and f_{O2}=307MHz

SNR is specified under no boost conditions. Also, input referred noise density measured at ω_o is $10\,nV/\sqrt{Hz}$ and $24\,nV/\sqrt{Hz}$ for 24dB and 0dB boost setting, respectively. Filter consumes power of 43mW. The experimental results are summarized in Table 2.3:

Table 2.3 Measurement results for Gm-C equalizing filter

Parameter	Value
Bandwidth at no boost	330MHz
Maximum Boost	25dB
Power	43mW
IM3 (Boost=0dB)	-41dB
Output Swing	250mVp-p
SNR (Boost=0dB)	49dB
Technology	0.35µm
Total Area	$0.5mm^2$

2.6 Equalizing Filter Design Using LC Techniques

Proposed biquad based implementation of the equalizing filters can be pictorially viewed as in Fig. 2.20.

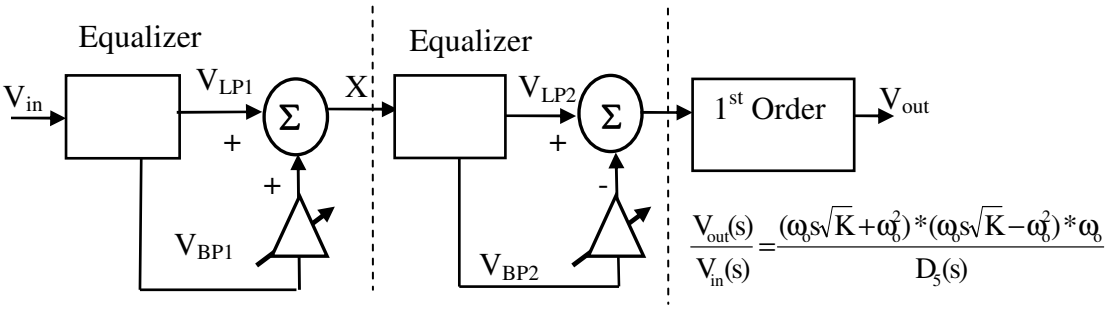
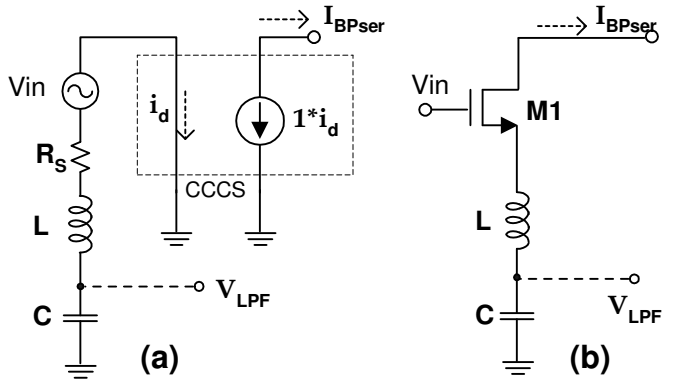


Fig. 2.20 Biquad based implementation of the equalizing filters

These signals are summed progressively to realize a pair of real zeros. To implement the equalizer sections shown in Fig. 2.20, both 2nd order lowpass and bandpass signals are required. While concurrent availability of bandpass and lowpass signals in a Gm-C biquad renders the implementation of the boost architecture in Fig. 2.20 simple, the LC implementation calls for certain creative modifications. The traditional parallel LC section used to realize a bandpass function is not amenable to generate lowpass signals (current through parallel R-L-C resonator is bandpass; to generate lowpass voltage, this current needs to be integrated at cost of additional hardware). However, considering a series resonator prototype such as one shown in Fig. 2.21(a), it can be seen that it generates both bandpass and lowpass signals, albeit in different domains. The current flowing through the series LC resonator (I_{BPser}) is bandpass in nature; while the capacitive element C integrates this current to generate lowpass voltage signal (V_{LPF}).



$$V_{LPF} = \frac{1/LC}{s^2 + sR/L + 1/LC} Vin \qquad I_{BPser} = \frac{s/L}{s^2 + sR/L + 1/LC} Vin$$

Fig. 2.21 (a) Series resonator prototype (b) Transistor implementation of (a)

An active implementation of such series resonator prototype that uses just one transistor is shown in Fig. 2.21(b). Transistor M1 serves for multiple operations: it generates the bandpass current, acts as a buffer for the input and provides termination for the series resonator. The fact that Butterworth transfer function requires a low Q value further validates the choice of LC prototype with M1 acting as the intentional loss for the resonator.

For actual implementation of the 5th order Butterworth filter with equalizing zeros, the two series-resonator based LC equalizer sections are cascaded. A simplified single-ended version of the complete LC filter that realizes fifth order Butterworth function is shown in Fig. 2.22. Currents from transistors M1 and M3 (I_{BPF}) are required to be variable for programmability of equalization gain. This is achieved by variable gain Gilbert-cell based current attenuators A_1 and A_2 controlled through V_B. The real pole at the 1st biquad output is pushed to 3GHz by using a negative capacitor -$C_{n.}$ which is designed to counter the parasitic and common-mode detector capacitance at the output node of the 1st biquad (C_3). Ignoring the parasitic capacitance Cp and using node equations at V_{O1} and V_{OUT}, the complete transfer function $H(s)=V_{OUT}(s)/V_{IN}(s)$ can be written as:

$$H(s) = \frac{(sC_1 + gm2)}{s^2 L_1 C_1 + s\frac{C_1}{gm1} + 1} * \frac{(sC_2 + gm4)}{s^2 L_2 C_2 + s\frac{C_2}{gm3} + 1} * \frac{1}{1 + sC_3 R_1} * \frac{1}{1 + sC_4 R_2} \qquad (2.12)$$

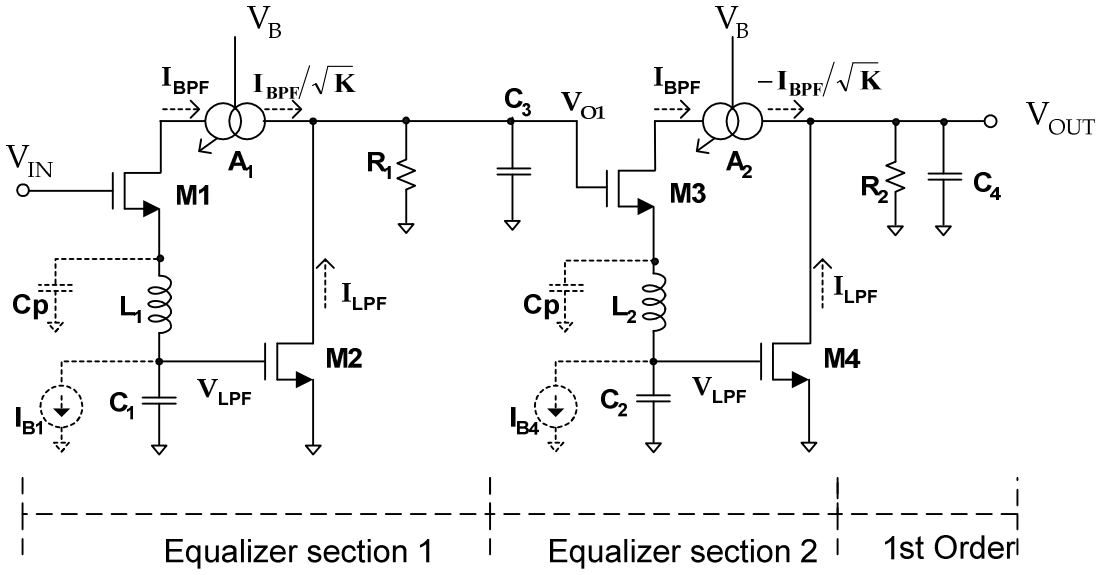


Fig. 2.22 Simplified schematic of the 5th order Butterworth filter

2.7 Summary of Experimental Results for LC Equalizing Filters

The prototype for 1GHz equalizing filter [3] was fabricated using TSMC 1P6M 0.18µm standard CMOS technology. Thick Metal-6 layer is used for inductors. Test setup, similar to one described earlier in this chapter for OTA-C boost filter, is used to characterize this filter. Magnitude plots, thus obtained, are shown in Fig. 2.23. A maximum boost gain of 23.6dB is achieved. The filter displays -3dB frequency (under 0dB boost) of 1.15GHz while consuming 72mW of power.

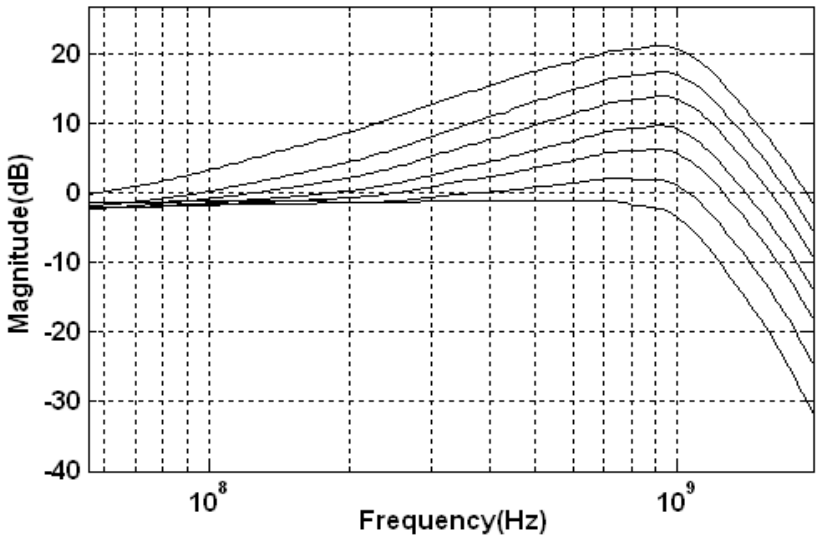


Fig. 2.23 AC magnitude across 0-23.6dB boost measured for 1.1GHz LC boost filter

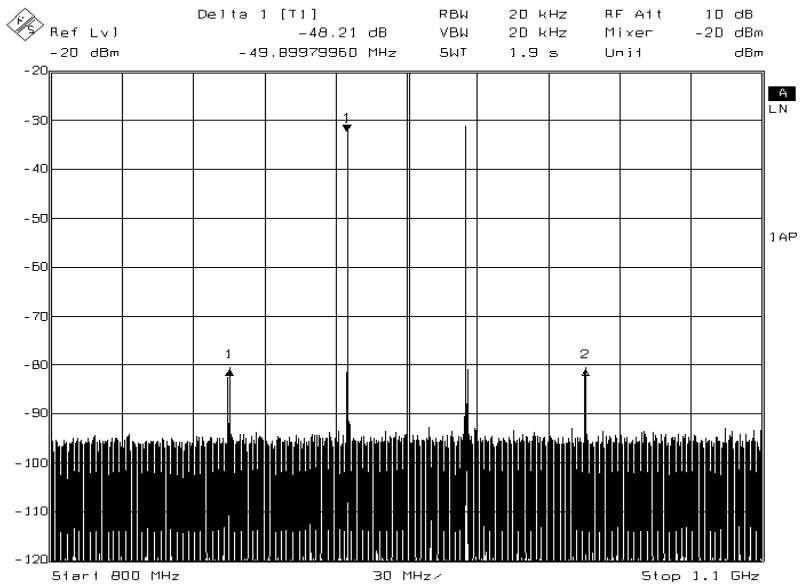


Fig. 2.24 Measured intermodulation distortion for 1.1GHz LC boost filter

For a two tone input (250mV p-p with tones at 925MHz and 975MHz), third order intermodulation distortion (IM3) of -48dB is observed for 0dB boost setting (shown in Fig. 2.24). Measurement results also show SNR of 47dB. Table 2.4 outlines the experimental results.

Table 2.4 Measurement results for the LC equalizing filter

Parameter	Value
Bandwidth (0dB boost)	1.23GHz
Maximum boost	24dB
Power	72.2mW
IM3 at 0dB boost	-48.2dB
Output swing	250mVp-p
SNR at 0dB boost	47dB
Total area	1.38mm^2

The discussion included here has been limited to a brief overview of the LC topology and its comparisons to Gm-C based approach. Further details about design of the equalizing LC filter can be found in [3].

2.8 Gm-C vs. LC Structures for Equalizing Filters

Appropriate choice of filter topology: Gm-C or LC is crucial for a design optimized for power and (or) area. For low and very high bandwidths, obvious architectural choices are Gm-C and LC respectively. Careful analysis needs to be performed to weigh relative merits of these topologies for bandwidths in mid frequency range. It can be appreciated that the active elements used to emulate an inductor in a

Gm-C resonator section would make these filters noisier (or less power efficient) than their LC counterpart. However, area constrains in realizing passive inductors for filters in few hundreds of mega-hertz range rule out the use of LC prototypes for such frequencies. Thus, the choice of topology for a high frequency filter: LC or Gm-C depends heavily on frequency of operation, SNR requirement and area constrains. These dependencies are hereby analyzed in context of equalizing LC and OTA-C biquadratic structures discussed above. The analysis has been kept generic enough to be extrapolated to other LC and OTA-C topologies.

2.8.1 Power and Noise Considerations

While comparing the power efficiency of LC and OTA-C prototypes *power-noise-product* which has been well elaborated upon in [3] is used as a benchmark. For simplicity a single equalizing section (instead of the whole filter) is considered. Considering the LC 'Equalizer Section 1' shown in Fig. 2.22, noise at node Vo1 (output of first equalizing section) is evaluated. Noise of active elements (M1, M2, R_1 and I_{B1}) is expressed in terms of V_{nGm2}^2 (input referred noise density of M2). A gain of 4 is assumed for the bandpass path (corresponding to a boost gain = 12dB per section, thus $gm_1=4*Q*gm_2$.). R_1 = 1/gm2 is assumed to ensure 0dB low frequency gain. Expressions for noise density due to lowpass path (V_{nLPF}^2) and bandpass path (V_{nBPF}^2) of the series-LC equalizer section (at node Vo1) are thus derived as:

$$V_{nLPF-LC}^{\ 2} = V_{nGm2}^{\ 2}\left|\frac{2\omega_o}{s+2\omega_o}\right|^2\left\{\frac{1}{4Q}\left|\frac{\omega_o^{\ 2}}{D(s)}\right|^2+\frac{1}{4Q}\left|\frac{\omega_o(Qs+\omega_o)}{D(s)}\right|^2+2\right\} \qquad (2.13)$$

$$V_{nBPF-LC}{}^2 = 4V_{nGm2}{}^2 \left|\frac{2\omega_o}{s+2\omega_o}\right|^2 \left\{\frac{1}{Q}\left|\frac{s\omega_o}{D(s)}\right|^2 + Q\left|\frac{\omega_o{}^2}{D(s)}\right|^2\right\} \tag{2.14}$$

where $D(s)= s^2+ \omega_o s/Q +\omega_o{}^2$ and Q is the *quality factor* of the biquad. the terms within the curly braces in (2.13) correspond to the noise contribution of M1, I_{B1} and M2 and R_L in that order and the terms within the curly braces in (2.14) correspond to the noise contribution of M1 and I_{B1} in that order. The total power consumed by the LC biquad can be expressed as: $P_{LC} = (2+4Q)*P_{Gm2}$ (as $gm_1=4*Q*gm_2$ and $R_1 = 1/gm2$), where P_{Gm2} is the power consumption of gm2.

Expressions for $V_{nLPF\text{-}GmC}{}^2$, $V_{nBPF\text{-}GmC}{}^2$ (noise density due to lowpass and bandpass path of the Gm-C equalizer section: Biquad 1 in Fig. 2.9) and P_{GmC} (total power consumed by Gm-C equalizer section) can also be derived in a similar manner [3]. Finally, the relative power efficiency of the LC equalizer section (η) is defined as the ratio of integrated power-noise product of Gm-C equalizer section to that of the LC one and is given by:

$$\eta = P_{GmC}\int_0^{\omega_0}\left(V_{nLPF-GmC}{}^2 + V_{nBPF-GmC}{}^2\right)d\omega \Big/ P_{LC}\int_0^{\omega_0}\left(V_{nLPF-LC}{}^2 + V_{nBPF-LC}{}^2\right)d\omega \tag{2.15}$$

To directly compare the power efficiency of LC series resonator based equalizing topology to the Gm-C one; η is plotted as a function of Q in Fig. 2.25. It is evident from the plot that the implemented LC series resonator based biquads (with Q=0.618 and Q=1.618) are on an average about 7.3 times more power efficient than Gm-C ones.

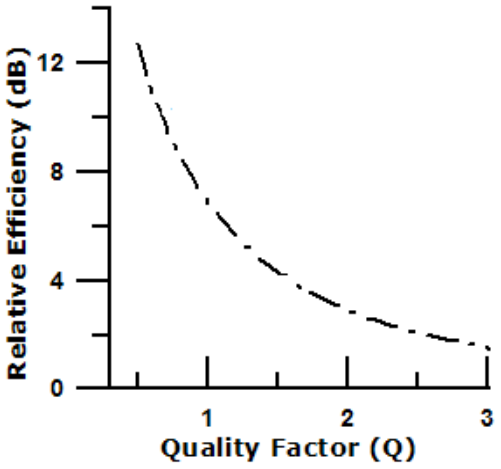


Fig. 2.25 Relative power efficiency (for LC and GM-C equalizing filter sections) versus quality factor

2.8.2 Area Considerations

Though LC filters are more efficient than the Gm-C ones; their area, especially at low frequencies and SNR, can be prohibitively large. To formulate area relations for LC and Gm-C filters as function of SNR and frequency, we depend on concepts of impedance and frequency scaling. Let A_{Co}, A_{gmo} and A_L be the total area occupied by capacitors, transistors and inductors of a LC equalizer section respectively for signal to noise ratio SNRo(47dB) and cut-off frequency fo(1.1GHz). C, L and gm values can then be projected as a function of SNR and f by applying impedance scaling and frequency scaling (for constant noise) respectively. Capacitor, transistor and inductor area scales roughly by the same factor as C, gm and L respectively. Thus area of scaled LC filter (as a function of SNR and cut-off frequency) can be expressed as:

$$\mathrm{Area_{LC}}(\mathrm{SNR},\mathrm{f}) = \mathrm{A_{Co}} * \frac{\mathrm{SNR}}{\mathrm{SNRo}} + \mathrm{A_{gmo}} * \frac{\mathrm{SNR} * \mathrm{f}}{\mathrm{SNRo} * \mathrm{fo}} + \mathrm{A_L}\left(\mathrm{Lo} * \frac{\mathrm{SNRo}}{\mathrm{SNR}} * \left(\frac{\mathrm{fo}}{\mathrm{f}}\right)^2\right) \tag{2.16}$$

If $\eta_{1,2}$ represents the value of η obtained for the two biquads (with Q_1=0.618 and Q_2=1.618), area of a corresponding Gm-C filter (as a function of SNR and f) can be expressed in terms of A_{Co} and A_{gmo} as:

$$\mathrm{Area_{GmC}}(\mathrm{SNR},\mathrm{f}) = \frac{1}{2}\sum_{i=1}^{2}\left[\mathrm{A_{Co}} * \frac{\eta_i(2+4\mathrm{Q_i})}{2(7+1/\mathrm{Q_i})} * \frac{\mathrm{SNR}}{\mathrm{SNRo}} + \mathrm{A_{gmo}} * \eta_i * \frac{\mathrm{SNR} * \mathrm{f}}{\mathrm{SNRo} * \mathrm{fo}}\right] \tag{2.17}$$

In 0.18μm technology, $\mathrm{Area_{LC}}$(46dB,1.1GHz) = 630Kμm^2 which is about twice of $\mathrm{Area_{GmC}}$(46dB,1.1GHz). However, from (2.13) and (2.14) it is projected that $\mathrm{Area_{GmC}}$ would outrun $\mathrm{Area_{LC}}$ beyond certain f for a given SNR and beyond certain SNR for a given f. Fig. 2.26 depicts this trend by plotting both the areas in K-μm^2 across SNR and f. For instance, at f=2GHz, $\mathrm{Area_{Gm\text{-}C}}$ equals $\mathrm{Area_{LC}}$ for SNR of 44dB and progressively more area for higher SNR. This trend suggests that the LC biquad can achieve much better power efficiency without area penalty at sufficiently high frequencies or SNR and vice-versa.

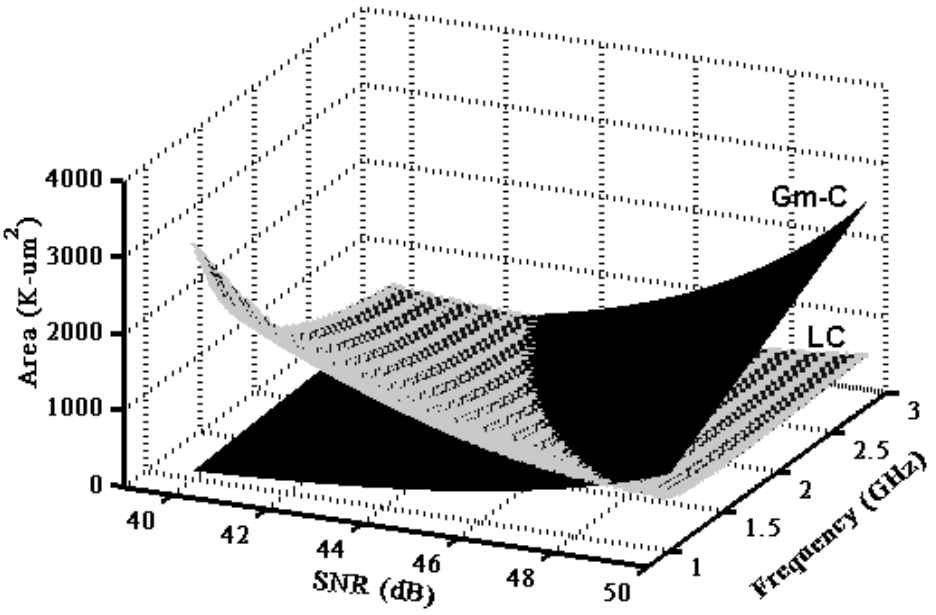


Fig. 2.26 Area comparison for Gm-C and LC equalizer section

Note that the above relations (2.16-2.17) are very generic and can be extended to any LC and OTA-C filter with corresponding substitutions for A_{Co}, A_{gmo} and A_L and η.

2.9 Conclusions

Increasing demand of high data rate systems has driven the rapid evolution of disk drive technology. Low power, high performance read channel systems have become critical for this development. This chapter analyzes one of the most important blocks for the read channel: an equalizing filter. Existing architectures for implementation of boost filters have been analyzed for their merits and demerits. An architectural solution that can be used to realize low power, high equalization gain wide-band filters has been proposed.

This chapter focused on power efficient design considerations and techniques for equalizing filters. With two specific examples of Gm-C and LC equalizing filters, architectural and design details are discussed and measurement results are presented for the corresponding prototypes. Gm-C and LC filters are examined for power efficiency and area requirements. Finally it leaves the readers with specific tools to analyze and directly compare relative merits of the two topologies to help them make prudent design choices based on the specifications.

It was shown that LC filters present a more power efficient alternative to Gm-C equalizing filters especially for high (multi GHz) bandwidth and high SNR. However, for typical applications cost of fabricating an LC filter in terms of mask and area may be prohibitive. Future works can explore the feasibility of all CMOS based wideband filters that can compete with LC architectures in terms of dynamic range and power efficiency. Lastly, this chapter concentrated on architectural and circuit solution to the problem of implementing high equalization gain in wideband filters with least possible power overhead. Programmability and tuning are not included in the shown implementation and can be a part of future research directions.

CHAPTER III

HIGH DYNAMIC RANGE, 1.3GHz, DUAL PATH CURRENT MODE FILTER

3.1 Introduction

3.1.1 Motivation

Power-efficient high-frequency continuous-time filters are desirable to support multi-Gb/s data communication in portable systems. The previous chapter presented two different approaches to realizing wideband filtering: a) Gm-C approach that relies on transconductor and capacitors as the basic signal processing elements to emulate inductors for implementation of the biquadratic filtering functions. b) LC approach that employs the integrated inductors available in the technology and uses them along with the capacitors as resonating elements. It was seen that the approach b) of using integrated inductors, in general, yields a more power-efficient design (less power consumption for given noise specifications). It was also discussed that this is a direct consequence of using passive frequency dependent elements (inductors) than emulating them through active blocks (transconductors).

However, use of integrated inductors entail certain disadvantages that may make this approach less lucrative for typical applications. Firstly, integrated inductor based filters typically occupy higher area than Gm-C filters for the applications discussed so far in this dissertation. It was shown, in the last chapter, that for progressively higher bandwidths (multi-GHz) and high SNR, LC filter area can potentially be competitive

against Gm-C filters. For bandwidth roughly around one GHz and SNR ~ 50dB, a Gm-C filter is expected to occupy far less area than its LC counterpart. Another disadvantage of using integrated inductors for filtering stems from the fact that realization of inductor as a component may require additional mask and or processing step for fabrication (requires a low resistivity metal layer). Standard CMOS technologies typically do not offer high quality inductors as an available component. This can be a deterrent for system implementations where inductors are not required for any other analog processing block (especially when there is no integrated RF sub chain). Lastly, integrating inductors involve increased complexity due to electromagnetic considerations.

For the above stated reasons use of inductors to realize high frequency filters may not be desirable in many circumstances. Use of Gm-C filters at high frequency, however, comes at a cost of significant power consumption. Focus of this research is to significantly improve power efficiency of such Gm-C filters. Apart from architectural efficiency, the power-efficiency of a Gm-C filter is limited by that of its basic building block, the operational transconductance amplifier (OTA).

The power-efficiency of an OTA can be defined in terms of a ratio of the signal-to-noise power ratio (SNR) to the power dissipation for a specified transconductance (gm) and minimum distortion performance. The relationship between power-efficiency and noise is a direct one and was explored in the proceeding chapters. An efficient transconductor would yield in minimum noise for a given signal gain (transconductance). Thus, power efficiency of a transconductor can be expressed as

'power-noise-product' as described earlier. Alternately, it can also be quantified using input referred noise for different transconductors that have same power consumption.

Power efficiency also depends on the linearity of the transconductor, albeit indirectly. Since distortion performance relies heavily on the input signal amplitude, linearization of the OTA plays an important role in improving its power efficiency. For instance, for a certain specified third-harmonic distortion to amplitude ratio (HD3) of a differential pair OTA, given by $Vi^2/(32*V_{GST}^2)$ (where Vi is the input signal amplitude and V_{GST} is the overdrive voltage of the transistor), signal amplitude can be doubled if the linear range has been extended by a similar factor. That is, Vi can be increased by a factor of 2 if V_{GST}, and hence the power consumption, is increased by the same factor. Thus, SNR (defined as power ratio of signal to noise) improves by 6dB at the cost of doubling the power consumption, which represents a power efficiency improvement by a factor of 2. This is clearly an advantage over noise reduction through impedance scaling, where the SNR improves only by 3dB when the power consumption is doubled: which leaves power efficiency unaltered. A linearity improvement through mere increase in V_{GST}, however, is ultimately limited by voltage headroom and mobility degradation effects. This fact had spurred significant research in OTA linearization techniques over the past two decades [23-26].

3.1.2 A Case for Complementary Pseudo-differential Transconductor

A complementary CMOS inverter based structure can be used as an atypical transconductor when biased in its linear region. Application of this structure as a

transconductance element in high frequency filters was first reported by Nauta in [25]. It will now be shown that this complementary transconductor provides superior power efficiency as compared to a traditional plain vanilla transconductor: a differential pair.

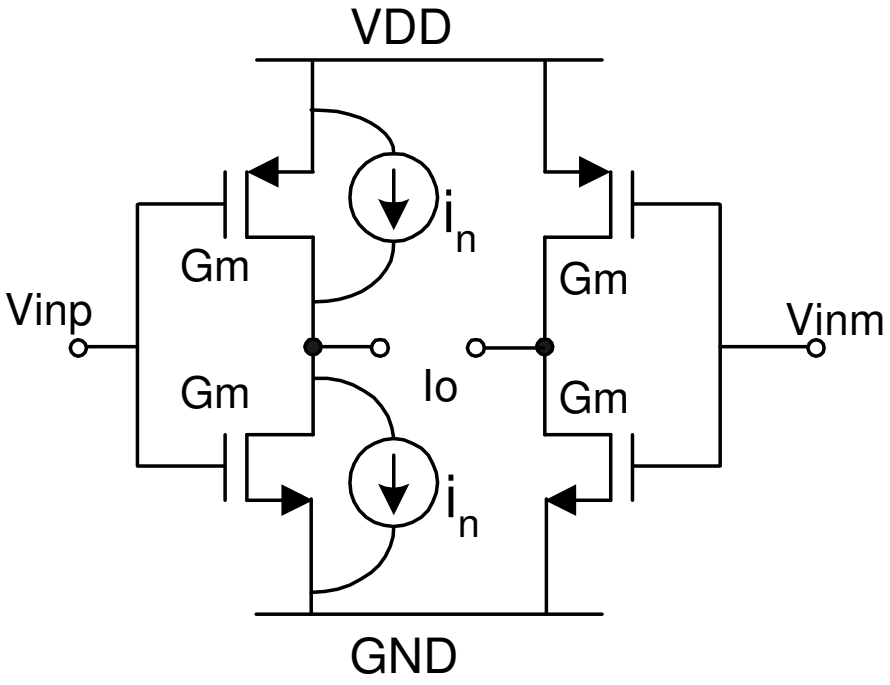


Fig. 3.1 Complementary devices based transconductor as used by Nauta

Comparing the CMOS inverter based Nauta's transconductor (Fig. 3.1) to a simple differential pair (Fig. 3.2) following observations can be made:

A) The supply current for this transconductor is re-used between NMOS and PMOS device drivers resulting in higher gm for the given power and the output noise compared to OTA schemes that use only NMOS or PMOS as transconductor. This

implies four times lower input referred noise for given power consumption. Let the transconductance of each of the transistors be gm. Also assuming that each of these transistors contributes noise current of i_n, the input referred noise voltage for transconductor in Fig. 3.1 is given by:

$$v_n^2 = \frac{2i_n^2}{4gm^2} \tag{3.1a}$$

However, for a differential pair based transconductor shown in Fig. 3.2, corresponding input referred noise is given by:

$$v_n^2 = \frac{2i_n^2}{gm^2} \tag{3.1b}$$

From the expressions shown in (3.1), it can be concluded that for given transconductance gain, input referred noise for the differential pair is four times higher than that of the complementary transconductor. This corresponds to a factor of 4 power-efficiency improvement (assuming that same bias current is used to realize the similar transconductances in the two cells).

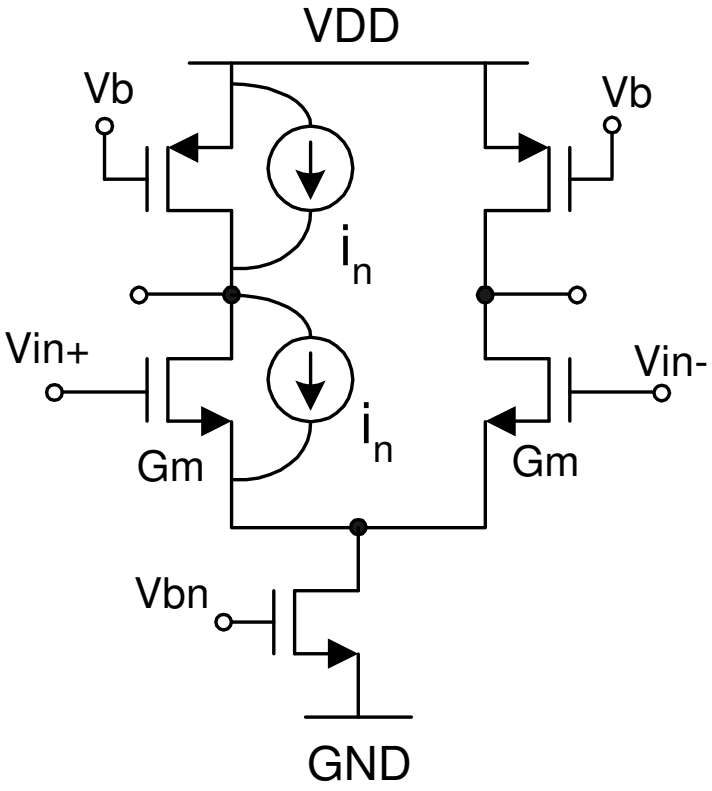


Fig.3.2 Differential pair based transconductor

B) Linearization is achieved through class-AB action and it works without reducing the overall transconductance of the structure. Higher linear range for the complementary Nauta's transconductor can be illustrated using gm-vs-I curves shown in Fig. 3.3. Transconductance of the complementary OTA doesn't roll off as sharply as that of a differential pair OTA. This can be explained due to the fact that signal current through the arms of differential pair is limited to the tail current. This is in contrast to the case of complementary Nauta's transconductor where current is limited by input voltage and supply levels only. Simulations of the best designed differential pair and

complementary OTA show that later supports 33% higher voltage swing for given HD3 owing to its superior Gm linearity.

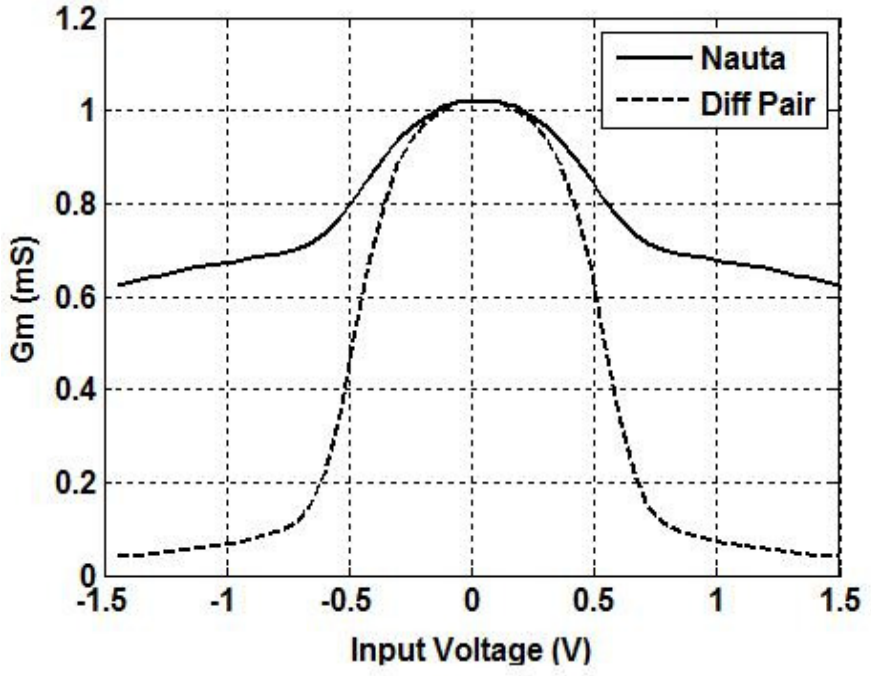


Fig.3.3 Gm variation as a function of input voltage

Taking into account the low-noise properties and the better linearity of the complementary transconductor it can be shown that this OTA provides about 7 times improvement in power efficiency over a traditional differential pair OTA, which other linearization schemes do not achieve (7~ $4*1.33^2$ – a factor of four due to improved noise for a given power and a factor of 1.33^2 due to improved linear range).

Note that, we have so far compared a complementary Nauta's transconductor to a simple differential pair. Any other linearized transconductor such as source degenerated

or multi-tanh schemes introduce additional noise due to linearization element or unequal division of noise from bias current source between differential pair respectively. Thus, it is sufficient to compare power efficiency of a Nauta's transconductor to that of a differential pair.

Differential-pair based complementary structures have also been used in [18] and discussed earlier in this dissertation (Fig. 2.10(b)). Such structures exhibit the advantage of improved noise properties over a simple differential pair. However, as with any differential pair, their linearity is limited (as compared to Nauta's transconductor) due to the presence of tail current source. Further, increased input parasitic and headroom requirements weigh unfavorably against the use of such structures in scaled CMOS technologies.

Although the complementary Nauta's OTA has excellent power efficiency, there are several practical problems associated with it. Firstly, power supply rejection ratio of this OTA is a paltry -6dB for $gm_N = gm_P$ (a formal derivation would follow in next section). Secondly, the bias current (and hence the transconductance) is a strong function of the threshold voltage (VT) of the transistors, the supply voltage and carrier mobility of the transistors. This results in large gm variation across temperature and process corners. Use of a low-dropout regulator as suggested in [25] is not effective in eliminating high frequency supply noise and would significantly reduce the power efficiency of the OTA.

Table 3.1 outlines the comparison between a differential pair based transconductor and a complementary Nauta's transconductor.

Table 3.1 Comparison between differential pair and Nauta's based transconductor

Parameter	Differential Pair OTA	Nauta's OTA
Input referred noise power	$v_n^2 = \frac{2i_n^2}{gm^2}$	$v_n^2 = \frac{2i_n^2}{4gm^2}$
Linear Range (1% HD3) 130nm CMOS, 1.2V supply	250mV	330mV
PSRR (from VDD) (low frequency)	gm/g_{OP}	gm_N/gm_N+gm_P

This research presents a new building block that retains the linearity and noise benefits of the complementary Nauta's OTA while side-stepping the above-mentioned issues associated with it. Finally, a 1.3GHz, 4th order Butterworth filter, fabricated in UMC's 0.13μm CMOS technology and designed using the proposed building block is presented. It is shown that the power efficiency using the proposed approach is significantly better than the state-of-the-art Gm-C filters.

3.2 Basic Building Block: A Complementary Current Mirror

It was shown in the last section, that though Nauta's transconductor has excellent dynamic range, it finds limited applicability due to high sensitivity to supply noise and VT variations. Poor supply rejection of this structure can be easily visualized using its small signal equivalent model shown in Fig. 3.4. Transconductance gain of supply noise is analyzed by 'grounding' the input at the gate port while uncorrelated supply-noise

signal is applied at VDD and GND which are sources of PMOS and NMOS transistors respectively. The supply noise present at VDD and GND appears at the output with the transconductance gain of gm each, where gm is the transconductance associated with the PMOS and NMOS drivers individually. It can be inferred that such pseudo differential structures, where source of the MOS driver transistor is directly connected to the noisy supply nodes and input signal voltage is applied to the gate, exhibit poor supply rejection. In this particular case, transconductance gain through either of the supplies is gm while the transconductance signal gain is 2gm. Thus power supply rejection ratio is given by:

$$\text{PSRR} = \frac{\text{Supply Noise Gain}}{\text{Signal Gain}} = \frac{\text{gm}}{2\text{gm}} = 0.5 \ = -6\text{dB} \tag{3.2}$$

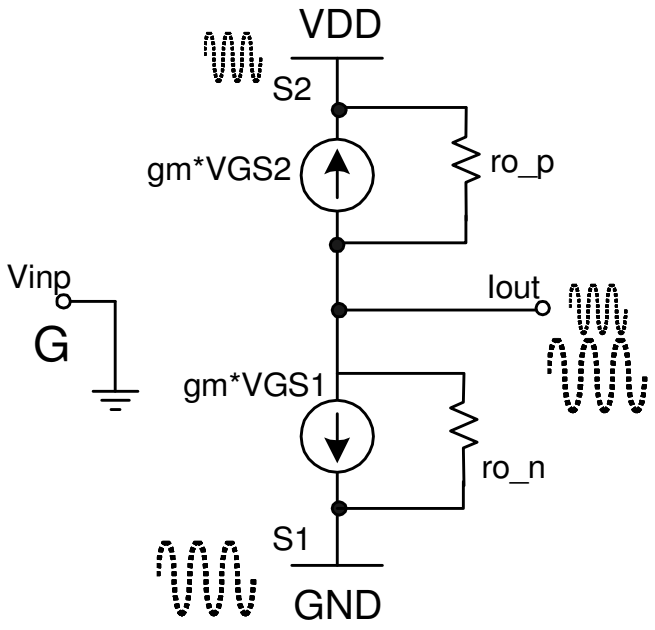


Fig. 3.4 Small signal model for Nauta's transconductor showing supply paths

3.2.1 Complementary Current Mirror Structure

One possible way to generate signal currents independent of supply noise is by using current mirrors. Current mirrors do not commute supply noise through them as long as input signal current is independent of supply noise. To visualize this, a simple NMOS current mirror is shown in Fig. 3.5. The mirror is excited through signal current i_in. Assuming transistors with very high output impedances, the current flowing through M1 is independent of GND bounces. Hence, GND bounces appear un-attenuated at the gate of transistors such that output current i_out is only proportional to i_in and does not carry any component of GND bounce. In practice finite output impedance of transistors and parasitic capacitances degrades the supply rejection (especially at high frequencies). A well designed current mirror, nevertheless, provides sufficient power supply rejection for most analog applications.

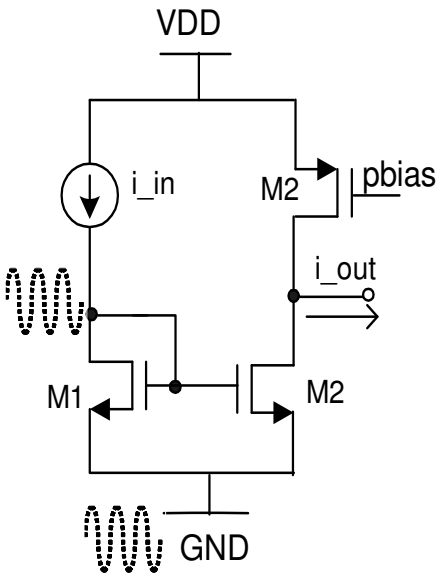


Fig. 3.5 Ground noise in a typical NMOS current mirror

Nauta's transconductor can be adapted as a complementary current mirror, using a possible implementation shown in Fig. 3.6. It can be seen that, although it is a current mirror configuration, it is not immune to supply noise as the gates of PMOS (M2) and NMOS (M1) are physically tied together. Hence, VDD noise appears at the gate of M1 and VSS noise appears at the gate of M2, resulting in supply noise being present at the output.

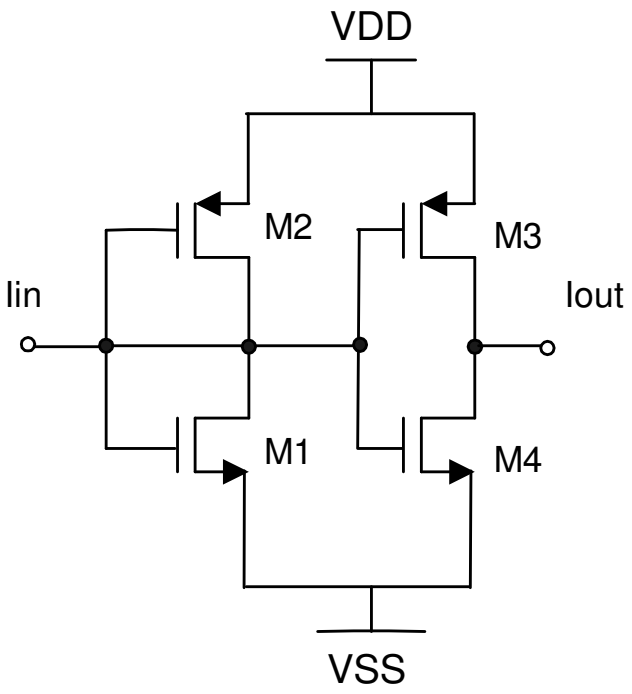


Fig. 3.6 Current mirror implementation of Nauta's structure

In order to make the output current of complementary transconductor independent of supply noise, perturbations at VDD need to be coupled onto the gate of the PMOS (M2) and the noise at ground onto the gate of NMOS (M1). This necessitates

that the NMOS and PMOS gates are not to be tied together. Coupling of the noise present at the supply to the respective gates can be achieved if the two load transistors (M1 and M2) are isolated into independent branches and are biased through current sources. The modified structure in this case evolves to the one shown in Fig.3.7. Note that signal currents i_in1 and i_in2 are in-phase (and not differential) input currents. Transistors M5 and M6 conduct a fixed DC current and are biased through pbias and nbias respectively.

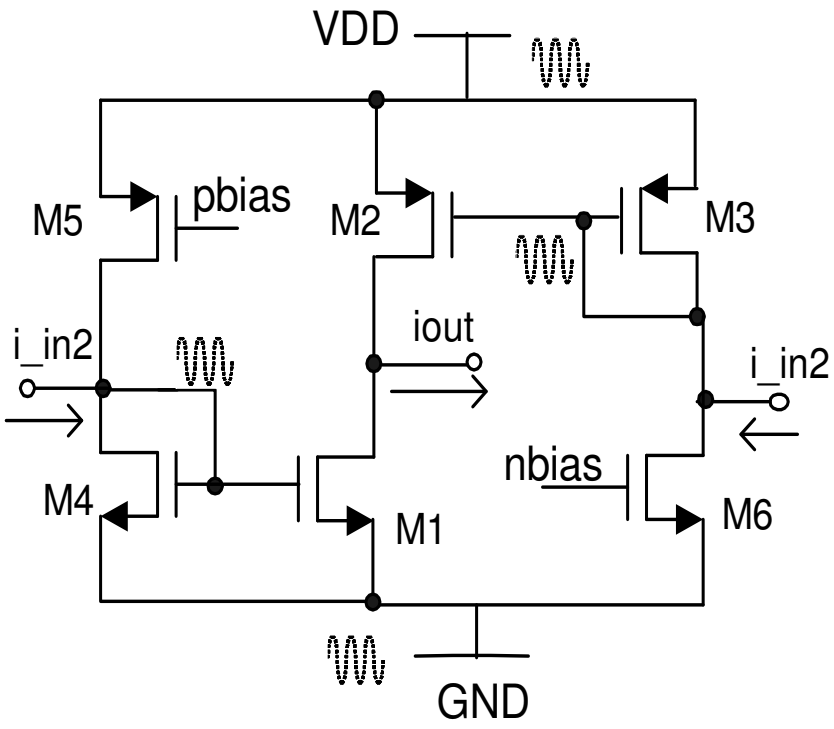


Fig. 3.7 Current biased complementary mirror

Mirroring action between M4 and M1 and also between M3 and M2 ensures that the PMOS gates of M2 and M3 carry the noise voltage present at the supply VDD and

the NMOS gates of M4 and M1 carry the noise present at GND. The output current iout is free from supply noise and is directly related to input current (i_in1=i_in2) through mirroring ratio. Note that signal commutation in this building block is in current mode. In principle, the basic building block is analogous to a current mirror and not a transconductor. Thus, through a complementary current mirror based structure shown in Fig. 3.7, improved supply rejection is achieved as compared to a complementary transconductor. Further, since the bias current of this structure is controlled through pbias and nbias, operating point of this structure is not as sensitive to VT and process variation as that of a complementary Nauta's transconductor. However, it remains to be seen whether the complementary current mirror structure of Fig. 3.7 can be easily adapted for the implementation of wideband filters. Also, the linearity performance of this structure vis-à-vis a complementary transconductor needs to be ascertained.

It is instructive to intuitively examine the linearity and noise properties of the structure in Fig. 3.7. This structure can be viewed as a cascade of two functional stages. While M4 and M3 convert the incoming current to a signal voltage, M1 and M2 form an equivalent complementary transconductance stage that generates the output current. Linearity and noise properties of the transconductor formed by M1-M2 are comparable to Nauta's due to complementary action. However, since M3 and M4 are biased through fixed current source (M5 and M6), linearity and noise of current to voltage (I-V) conversion is limited to that of an ordinary diode–connected load. For example, device M5 contributes to the noise accumulated at node i_in2 without participating in I-V conversion at this node.

In order to improve overall noise and linearity close to that of a true complementary structure, both PMOS and NMOS devices should participate in I-V conversion (complementary signal processing in current mirrors would yield wider dynamic range [27]). Thus PMOS M5 and M6 should sink in parts of the signal currents i_in1 and i_in2 respectively without having to physically connect their gates to input ports. In order to isolate GND noise from all PMOS gates and yet let M5 participate in I-V conversion, gate of M5 is tied to M3 gate (i_in2) and gate of M6 is tied to M4 gate (i_in1). This results in a structure shown in Fig. 3.8.

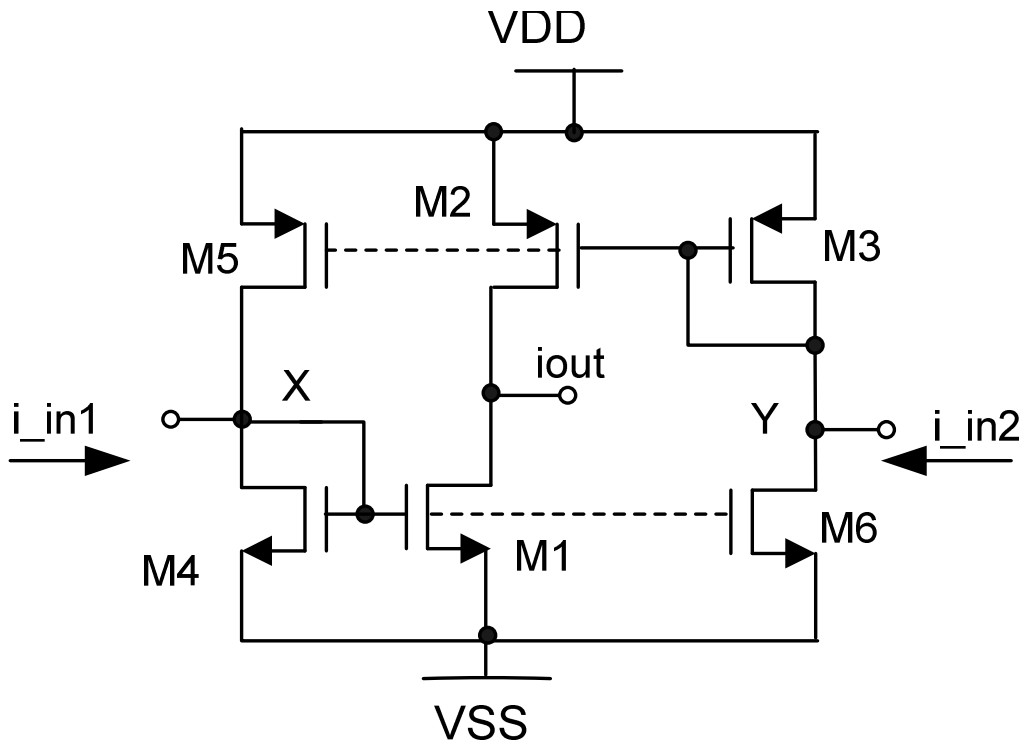


Fig. 3.8 Modification of structure in Fig. 3.7 for complementary operation

3.2.2 Small Signal Model of the Complementary M*irror*

Fig. 3.9 shows the small signal equivalent for the structure shown in Fig. 3.8. Output impedance of devices M3-M6 and M4-M5 are lumped into ro. Transconductance of NMOS devices (M4, M6) and PMOS devices (M3, M5) are denoted by gm_N and gm_p respectively. The mirroring ratio for the current mirror is chosen to be K (ie. gm1 = Kgm_N and gm2 = Kgm_P).

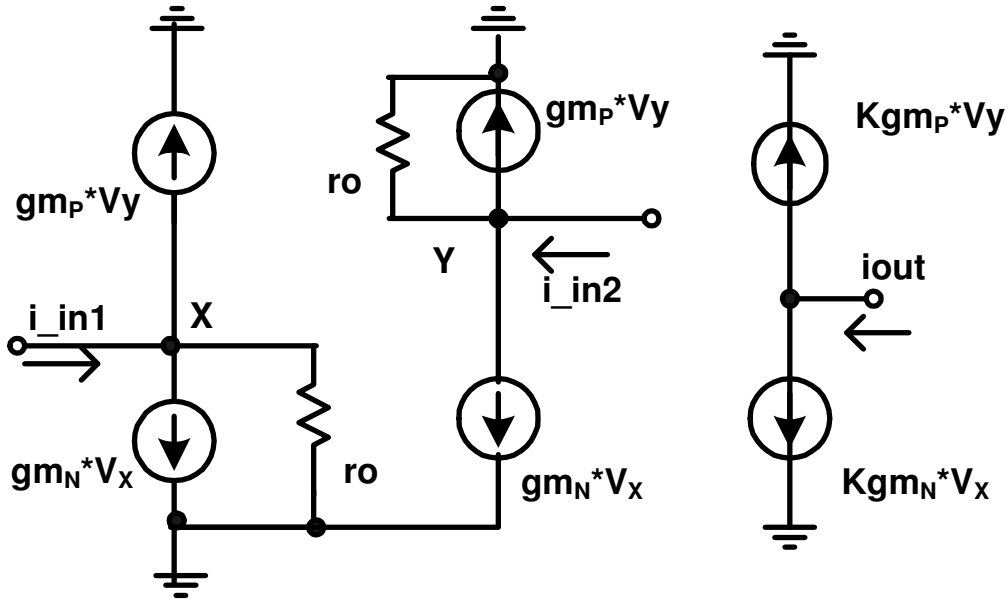


Fig. 3.9 Small signal model for the complementary structure in Fig. 3.8

From the small signal model shown in Fig. 3.9, following relations can be formulated:

$i\_in1 = gm_p\, Vy + gm_N\, Vx + Vx/ro$ (3.3)

$i\_in2 = gm_p\, Vy + gm_N\, Vx + Vy/ro$ (3.4)

$iout = Kgm_pVy + Kgm_NVx$ (3.5)

That is,

$$i\_in1 - i\_in2 = (Vx-Vy)/ro \tag{3.6}$$

$$i\_in1 + i\_in2 = 2gm_pVy + 2gm_NVx + (Vy + Vx)/ro \approx 2gm_pVy + 2gm_NVx \tag{3.7}$$

For $gm_p=gm_N$, following can be written:

$$iout = K\frac{2gm*ro}{1+2gm*ro}(i\_in1 + i\_in2) \approx K(i\_in1 + i\_in2) \tag{3.8}$$

Thus, the proposed structure mirrors the in-phase component of input currents (i_in1, i_in2), while the out of phase component is not mirrored to the output port. For in-phase input currents i_in1=i_in2 signal voltages Vx and Vy are identical and so are the currents flowing through devices M3-M6. Transistors M5 and M4 convert incoming current i_in1 to signal voltage Vx and transistors M3 and M6 convert incoming current i_in2 to signal voltage Vy. Signal voltages, thus produced, effectively isolate GND bounces and VDD supply noise onto NMOS and PMOS gates respectively. Also, I-V conversion is carried out in a linear fashion due to complementary nature of devices. Applying these voltages onto M2 and M1 gates yields an output current which is independent of supply and ground noise and matches the linearity and noise properties of a well designed complementary Nauta's transconductor.

For practical realization of structure in Fig. 3.8, further modifications are necessary. If connections (dotted) of Fig. 3.8 are indeed closed, one can see that DC bias for transistors M3-M6 is not well defined. At DC, transistors M3-M6 form a loop as in Fig. 3.10. The total accumulation at DC around the loop is 360 Degree (positive feedback). In practice, gain of such loop is less than unity due to finite go (output

conductance of transistor). Nevertheless, transistor bias currents for this structure cannot be determined reliably.

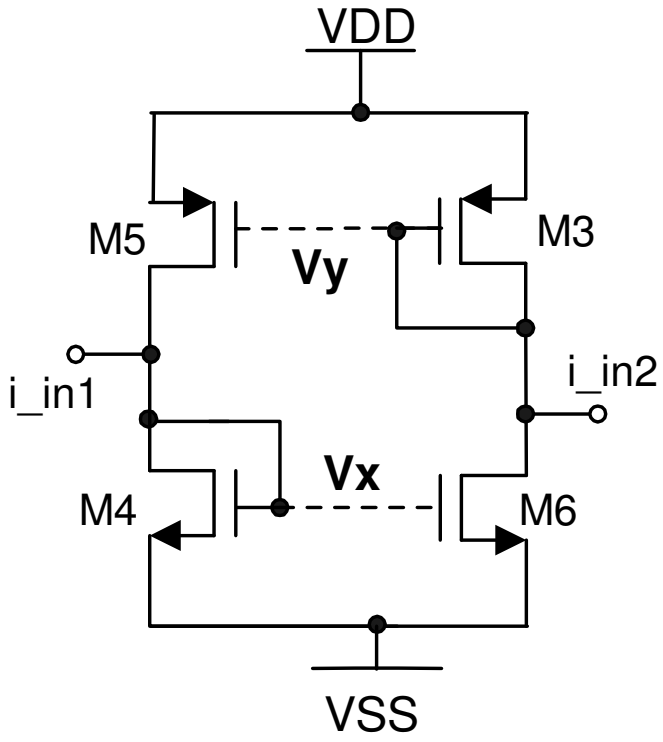


Fig. 3.10 Loop formed by mirror transistors

3.2.3 Proposed LRCM (highly Linear supply Robust Current Mirror) Structure

To eliminate the dependence of bias points on process parameters, the structure in Fig. 3.8 needs to be modified such that the loop is formed only for signal frequencies (and not at DC). Further, the bias point of the mirror transistors should be defined using independent current sources.

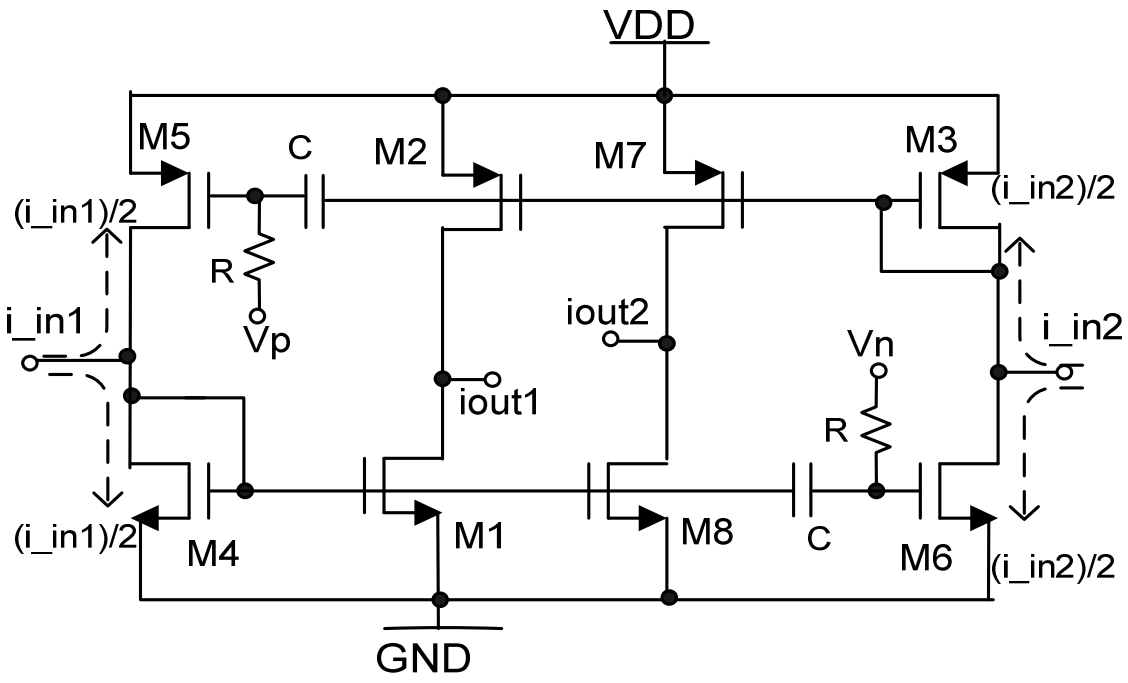


Fig. 3.11 Proposed highly linear, supply Robust Current Mirror (LRCM)

To this effect, the structure in Fig. 3.8 is modified to the one in Fig. 3.11 that shows the proposed LRCM (highly Linear supply Robust Current Mirror) structure. Here, the gates of M5 and M6 are capacitively connected to M3 and M4 respectively such that for signal frequencies >1/RC, signal swings at gates M3, M4, M5 and M6 are similar (as gm3=gm4=gm5=gm6); where gmi is the transconductance associated with transistors Mi. Thus, the input current i_in1(=i_in2) partitions equally between M4 and M5 (M3 and M6) as shown in Fig. 3.11.

Current to voltage conversion in the proposed structure is carried by M5-M4 and M3-M6 for the respective arms. The signal voltages, thus generated (at respective gates), are applied to the inputs of the transconductor formed by M1-M2. The gates of all PMOS carry VDD noise while the NMOS gates carry the noise from GND. Thus, the

generated output signal current is ideally free from supply noise. The DC bias for the structure is established through resistors R1 and R2: voltages vp and vn are generated by traditional current biasing. This ensures transconductances are independent of VT variations due to process and temperature. Since a dual path input current is essential for this complementary structure, an additional transconductor arm comprising of M7 and M8 is added to generate two copies of the output current, iout1 and iout2, that can be fed as inputs to a potential dual input next stage. For identical transconductance of all transistors and i_in1=i_in2, following can be stated for output currents:

$$iout1 = iout2 = i\_in1 = i\_in2 \tag{3.9}$$

It is important to note that the technique of processing signals using multiple paths does not affect the power efficiency as shown in [28]. Processing signals in multi-path circuits can be simply envisioned as splitting the main signal processing block into two parallel paths each of them providing half of the gain. This arrangement does not affect noise or the power of signal chain adversely.

It is interesting to note some of the properties of the loop formed by M3-M6 using Fig. 3.11. Observing the small signal equations (3.6-3.8), for conditions gm3=gm4=gm5=gm6=gm, following can be stated:

A) For in-phase input current (i_in1 = i_in2): The input impedance is given by 1/(2gm) looking in each of the ports.

B) For Differential current inputs (i_in1 = -i_in2): The input impedance offered by the structure is quite high (given by output impedance ro of the transistors).

Thus, the proposed LRCM block essentially rejects any out-of-phase current excitation applied to its dual input ports. This property has two important ramifications: Firstly, filter architectures constructed using LRCM block would have dual in-phase excitations, i.e., a pair each of input and output currents. Secondly, to construct differential architectures, an independent copy of structure would need to be used to process the differential counterpart. Differential filter architectures using LRCM blocks would be discussed later in this chapter.

For in phase input currents, the proposed LRCM block can also be represented as Fig. 3.12. Note that this is a single ended representation with i_in1 and i_in2 being in-phase currents. Pursuing the formal small signal analysis, it can also be shown that for signal frequencies >1/RC, GM_L = 2*gm3 = 2*gm4 and Gm_T = 2gm1 = 2 gm2.

For very low frequencies or DC, the signal present at the gate of M4(M3) (see Fig. 3.11) is not coupled to M6(M5). Hence the load transconductance GM_L is given only by NMOS or PMOS transconductance. That is, at signal frequencies <1/RC, Gm_L=gm3=gm4. This property has important ramification and would be revisited later in this chapter when implementation of filters using the proposed LRCM block is discussed.

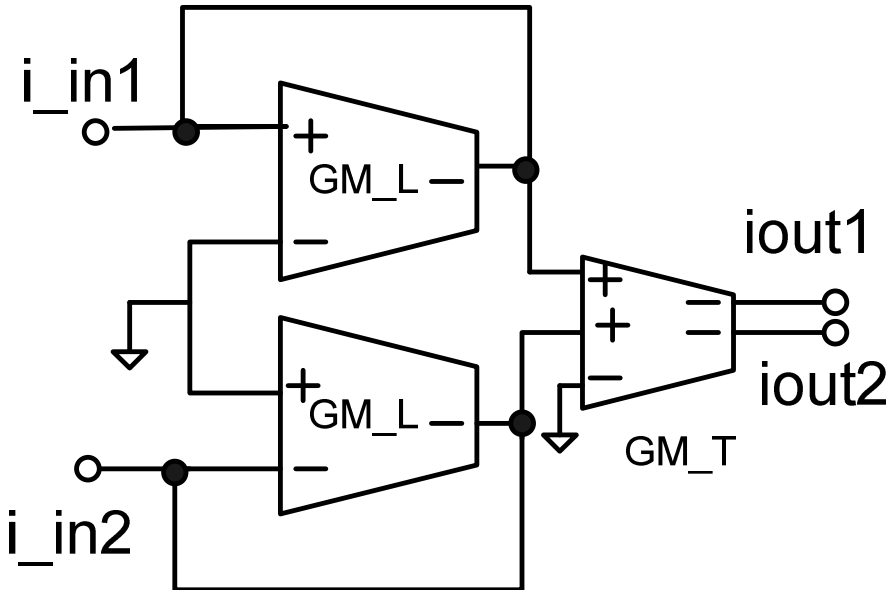


Fig. 3.12 Equivalent of the proposed dual path LRCM structure of Fig. 3.11 (for in-phase input currents)

The salient features of the proposed LRCM block are stated below:

1) Linearity: The linearity of this modified structure is similar to that of an equivalent Nauta's transconductor. The essence of this property lies with use of complementary transistors for signal processing. That is, both PMOS and NMOS participate in current to voltage and voltage to current conversion thus extending the linear range as shown earlier in this chapter and in [27]. For example, LRCM achieves HD3 of -70dB for peak to peak differential swing of 250mV with a current consumption of 1mA which is comparable to results obtained for equivalent Nauta's structure.

2) Noise: It was shown earlier in this chapter that power-noise efficiency (noise power for given signal swing and power) of a complementary Nauta's transconductor is 4 times better than a structure where only NMOS or PMOS participate in signal

generation. Correspondingly noise performance of the proposed LRCM structure is better than a simple current mirror. This can be formally shown by comparing the two structures (Fig.3.13 a-b) for same input signal current (i_in = i_in1+i_in2), voltage swing and mirroring ratio of 1. Transconductance of all transistors (gm) in Fig. 3.12 are assumed to be equal.

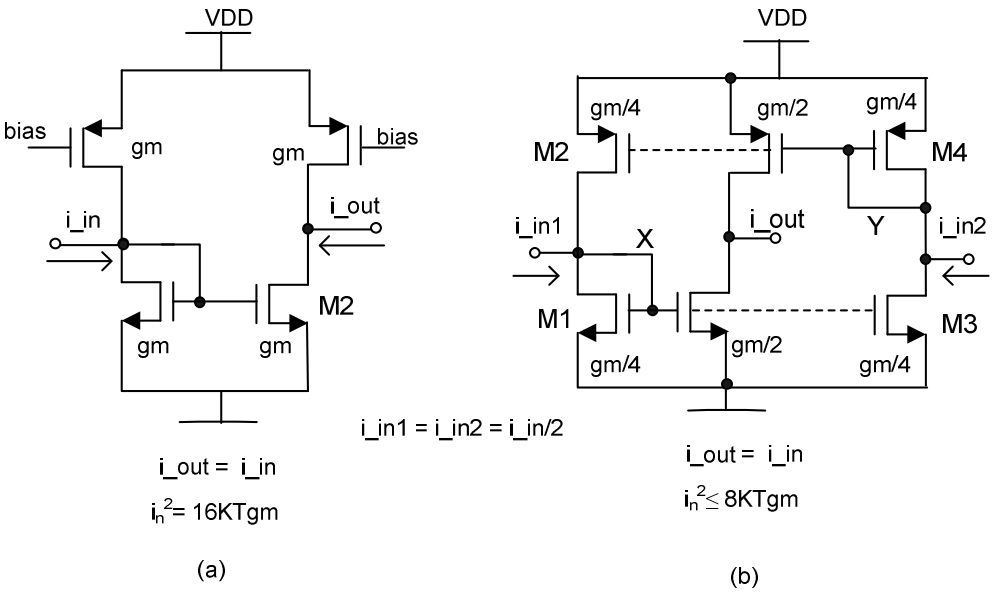


Fig. 3.13 Output current noise: (a) Simple current mirror (b) LRCM structure

For the simple current mirror, the output current noise is given by i_n^2 = 16KTgm. In the case of LRCM structure shown in Fig. 3.13(b), for the trivial assumption of in-phase noise current injected by M1-M2 and M3-M4 at nodes X and Y respectively, output current noise i_n^2 is given by 8KTgm. However, the noise current injected by M1-M2 at node X is not correlated to the current injected by M3-M4 at node Y. Since the

LRCM structure has been shown to reject out-of-phase input currents, the output current noise power is lower than 8KTgm. Further, the power requirement of the LRCM structure shown in Fig. 3.13(b) is two times lower than the simple current mirror shown in Fig. 3.13(a) due to lower valued transconductances. This, together with lower noise power yields a net power-noise efficiency improvement of at least 4 times.

3) Supply Rejection: The proposed building block has improved PSRR and is more robust to supply and VT variations that the complementary Nauta's structure. Specifically, low frequency transconductance gain from VDD for the LRCM structure is approximately go_p as against gm_p in case of Nauta's OTA, where gm_p and go_p refer to transconductance and output conductance of PMOS device. In simulations, low frequency supply rejection for the proposed structure is found to be -30dB as against -6dB for the Nauta's OTA (with similar device size and transconductance). It can be appreciated that supply rejection of the proposed LRCM structure is similar to that of a simple current mirror, relevant expressions pertaining to which are derived later in this section.

4) Lastly, this structure maintains a low voltage operation with headroom requirements even lower than that of inverter based Nauta's transconductor. The minimum supply requirement in case of proposed LRCM structure is VT + 2*Von+ Vswing, where VT, Von and Vswing refer to threshold voltage, transistor overdrive and signal swing respectively. The similarity of this structure to a digital inverter also ensures that the proposed LRCM structure can be integrated even as digital CMOS technology is scaled aggressively.

3.2.4 High Frequency Behavior of the Proposed LRCM Structure

The high frequency behavior of the LRCM structure can be analyzed by adding parasitic capacitance in the small signal model of Fig. 3.8. For simplification, it is assumed that capacitances at node X and Y are dominated by the respective gate capacitances. Thus, proposed LRCM structure exhibits a pole given by $\omega p = gm/Cnet$, where gm is the transconductance of the transistors (M3=M4=M5=M6) and Cnet represents the net capacitance at the mirroring node X (or Y) which mainly constitutes of gate capacitance of all NMOS (or PMOS) devices. In practice, this pole is absorbed in the intentional pole created at the input port when such current mirroring structures are used to realize filtering functions.

The parasitic capacitances also affect the supply rejection properties of the LRCM structure. Fig. 3.14 is the small signal model of the LRCM structure shown in Fig. 3.8, drawn to analyze current gain from VDD. To simplify the model, only relevant capacitances (ie. the ones connected to node Y) are shown. Gate capacitances of transistors M4-M6-M1 are clubbed into C1 while C2 constitutes of mainly junction capacitance at node Y. Output impedance of the PMOS and NMOS devices are indicated by ro_P and ro_N respectively. It can be seen that for $gm_P > 1/ro_P$, node Y carries the signal present at VDD ($Vy= V_{VDD}$) and hence output current is devoid of supply noise.

However, due to finite output conductance and node capacitance (C2), Vy deviates from V_{VDD}. To derive a wieldy expression, it is assumed that Vx does not carry any component of V_{vdd}. This is a fair assumption in light of the fact that that $Vy \approx V_{vdd}$ in the frequency of interest and $gm>1/ro_N$.

$$Vy = \frac{gm + 1/ro_P + sC1}{gm + 1/ro_N + 1/ro_P + sC1 + sC2} V_{VDD} \tag{3.10}$$

iout = -Kgm(Vy-V_{vdd})+V_{vdd}/(sC'+1/ro')

$$= Kgm\left(\frac{1/ro_N + sC2}{gm + 1/ro_N + 1/ro_P + sC1 + sC2}\right)V_{VDD} + \left(\frac{1}{sC'+ro'}\right)V_{VDD} \tag{3.11}$$

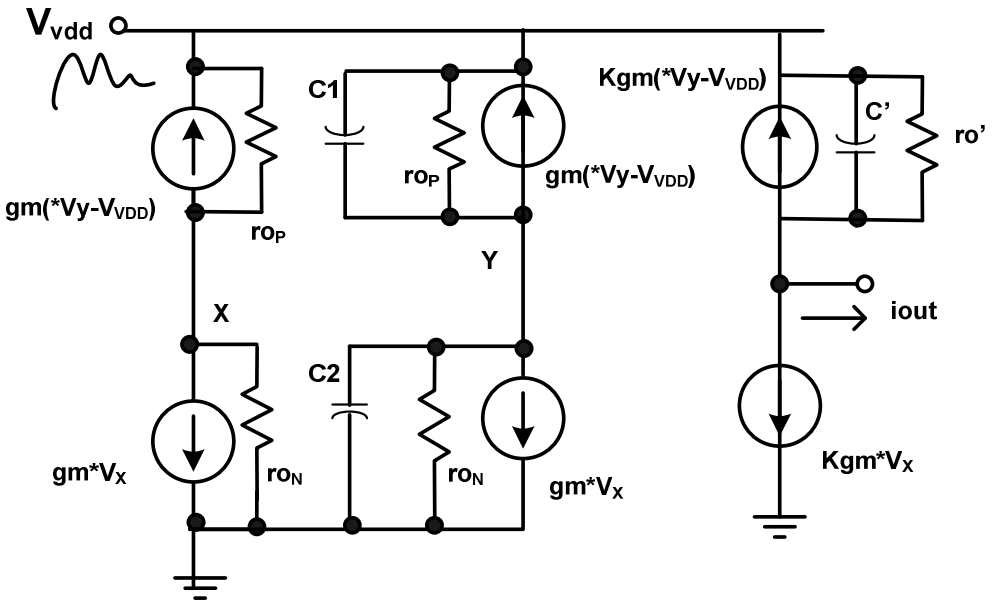


Fig. 3.14 Supply rejection from supply modeled for LRCM structure

3.2.5 Simulation Results for the LRCM Structure

Extensive simulations are carried at block level (LRCM structure) to verify its properties (linearity and supply rejection).

Input impedance of the LRCM structure shown in Fig. 3.11 is analyzed for in-phase (i_in1 = i_in2) and out-of-phase currents (i_in1 = -i_in2). Fig. 3.15 shows the plot for input impedance (Zin) of LRCM structure when in-phase current inputs are applied.

Here, i_in1 = i_in2 = i is applied to the input port and the voltage at the input terminal is observed and plotted as a function of frequency. As expected low frequency input admittance is given by 2*gm. For gm = 0.7mS, Zin = 684 ohms which is also indicated in the plot in Fig. 3.14. At higher frequencies impedance degrades due to the input pole (formed by 2gm and node capacitance). Input impedance of the LRCM structure for the out-of-phase inputs was simulated by applying out-of-phase current inputs. Input impedance for such inputs is found by on order 10Kohms. These simulation results relate well to the discussion in section 3.2 of this chapter.

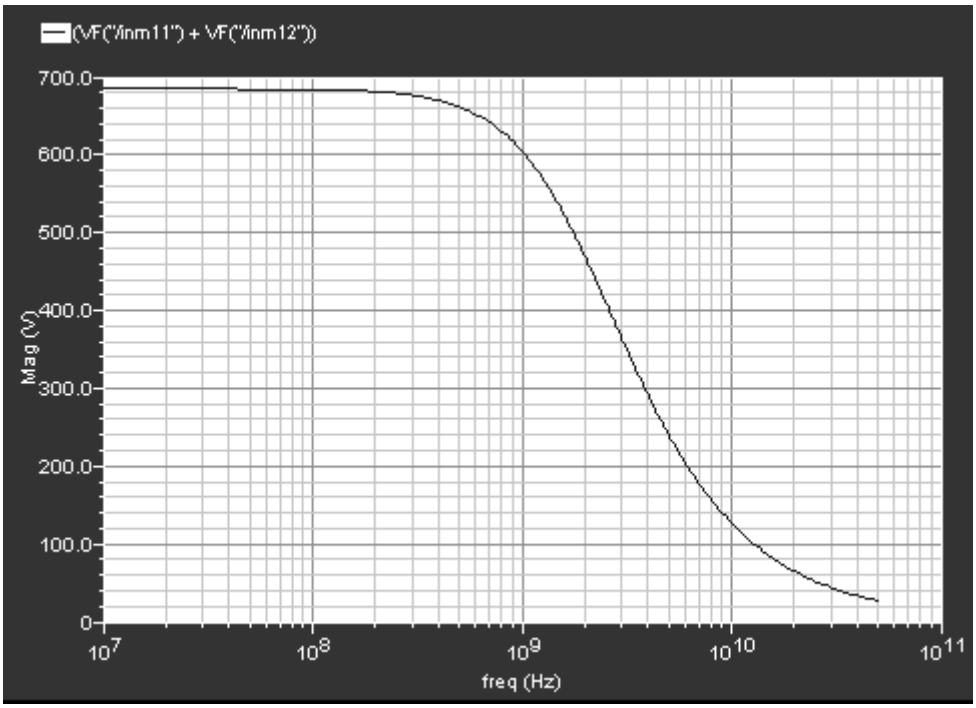


Fig. 3.15 Input impedance for in-phase current inputs to the LRCM block

The proposed LRCM structure has a high frequency pole at the input port as shown in section 3.2.4. The simulated magnitude response of the LRCM structure is shown in Fig. 3.16. The simulation is carried for a current mirroring ratio of 4 and the unity gain bandwidth of the structure is observed to be around 6.5GHz. Such wideband response is an important characteristic of this structure. This property proves to be quite useful when the filtering blocks are built using LRCM structures.

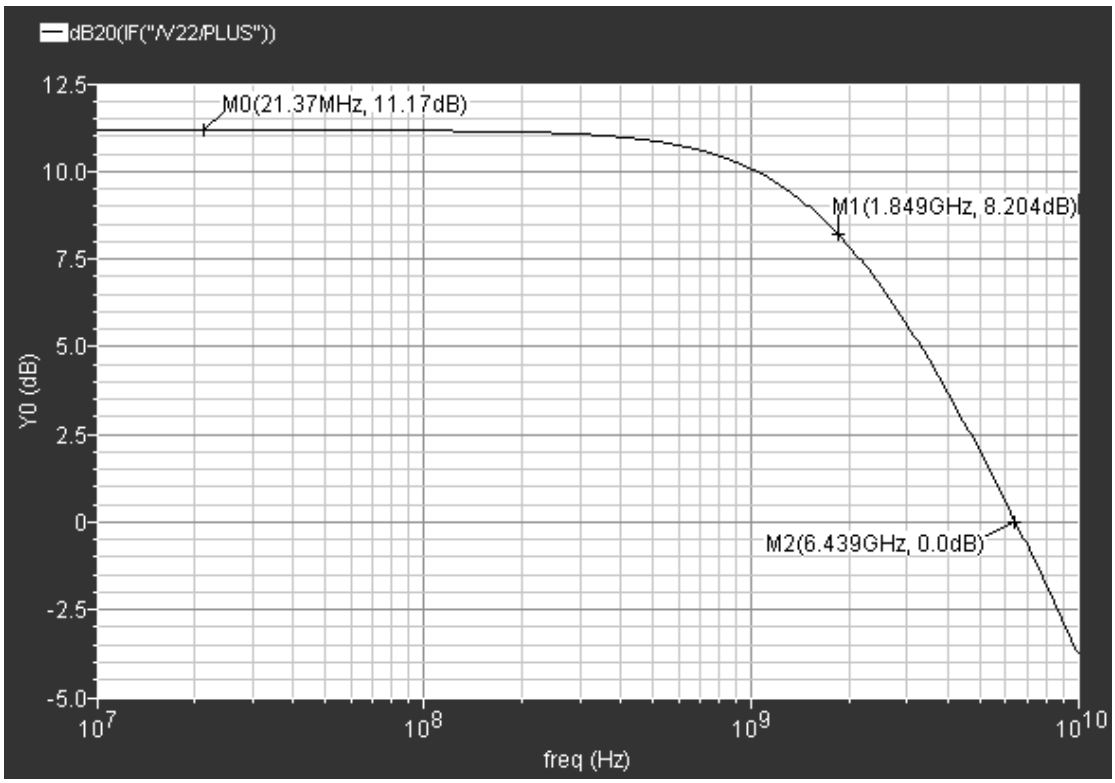


Fig. 3.16 Magnitude response of the LRCM structure

To verify the linearity properties of the LRCM structure, the in-phase input currents with frequency around 200MHz are applied to the ports. The current levels are

chosen such that the input voltage swing is around 220mV peak-peak. The output current spectrum is plotted in Fig. 3.17. As shown in the figure, the third order harmonic distortion is -67dB which is quite high for an open loop structure that does not use any external linearization.

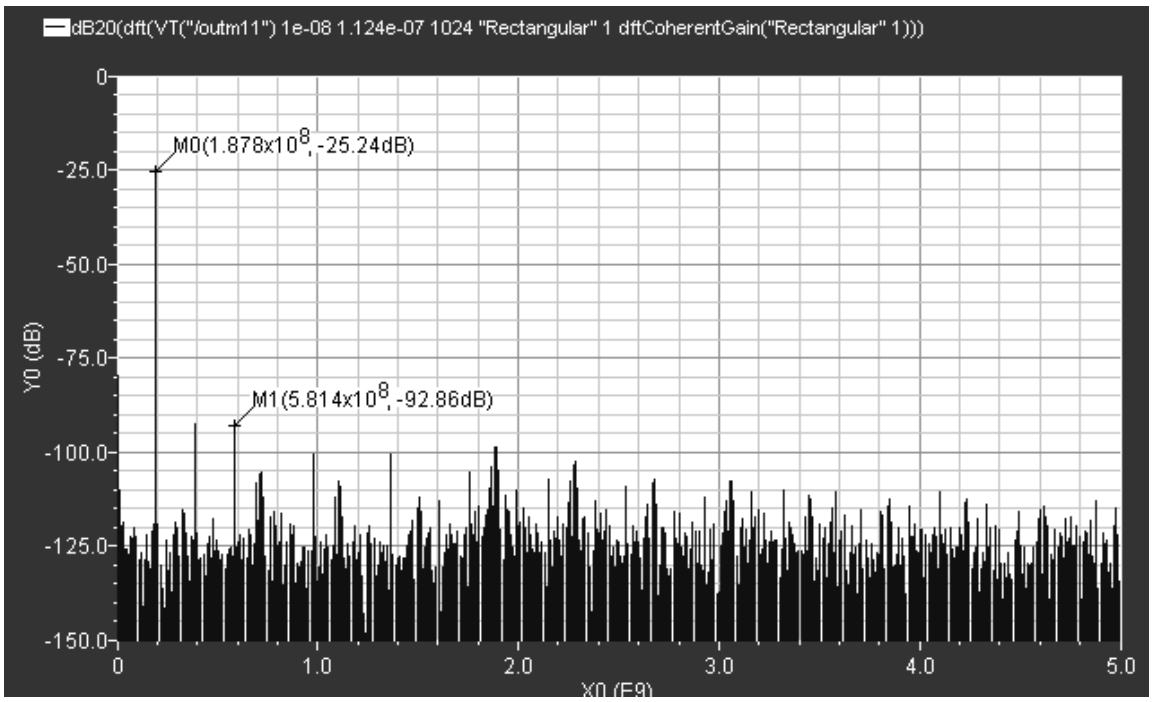


Fig. 3.17 Spectrum of the output current (LRCM structure)

Finally, to verify supply rejection properties of the LRCM structure, the signal is applied at the supply (VDD in this case) and the resultant output current is observed. The output current is normalized by the transconductance of the output stage (gm_T of Fig. 3.12). The resultant supply rejection plot is shown in Fig. 3.18. The low frequency supply rejection is simulated to be -32dB. In contrast, the supply rejection of a Nauta's

transconductor of Fig. 3.1 is a mere -6dB. These results agree well with the observations made in section 3.2.4.

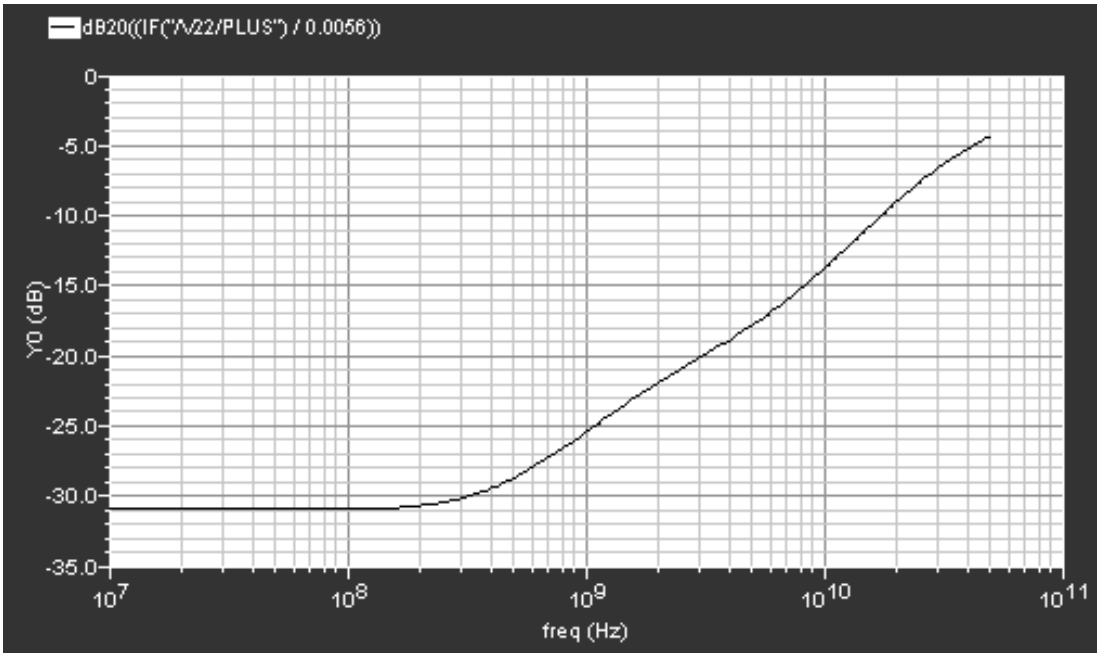


Fig. 3.18 Supply rejection of the proposed LRCM structure

3.3 Filter Design

Previous sections showed evolution of a linear Nauta's OTA to a linear current mirroring element that alleviates the drawbacks of Nauta's transconductor. This section describes the application of LRCM for design of wideband current mode filters.

3.3.1 Current Mode Filtering Techniques

In essence, the proposed LRCM structure can be viewed as a current mirror with vastly improved dynamic range. Better noise and linearity properties of this structure are

direct consequence of processing of signals through complementary devices. However, current mirroring properties are incidental to structural modification of the complementary OTA (Fig.3.1) to yield supply noise independent and process variations robust output. Due to inherent mirroring properties of the proposed LRCM structure, current mode filtering techniques are used to realize the wideband filter. Current-Mode techniques, in general, refer to designs where input and output signal relations are defined in terms of current variables. Current mode OTA-C filters are dual of voltage mode OTA-C filters [29]. In order to visualize this relation a current mode integrator is shown in Fig. 3.19(b) which can be derived by spatially arranging capacitive and transconductance elements of a voltage mode integrator shown in Fig. 3.19(a).

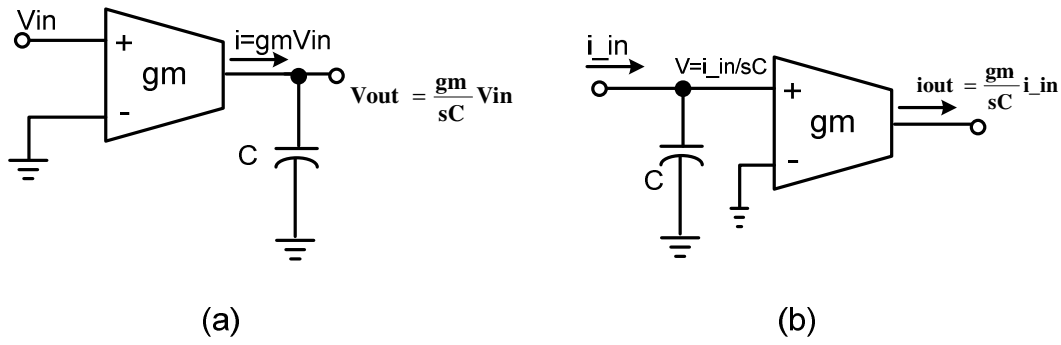


Fig. 3.19 OTA-C integrators: (a) voltage mode (b) transformation to current mode

A vast body of work has been reported on current mode filters [30-33]. Of Particular importance are architectures based on current mirrors or lossy integrators (that have low input impedance similar to the proposed LRCM structure). Fig. 3.20 shows the biquadratic section of such current mode filter using lossy integrating elements.

Transconductors Gm1-4 along with C determines filter's resonance frequency (ωo) while quality factor Q is determined by losses presented by Gm1 and Gm3. The expression for the output current is given by:

$$i\_out = \left(\frac{Gm2Gm5 / C^2}{s^2 + \frac{Gm1 + Gm3}{C} s + \frac{Gm1Gm3 + Gm2Gm4}{C^2}} \right) * i\_in \qquad (3.3)$$

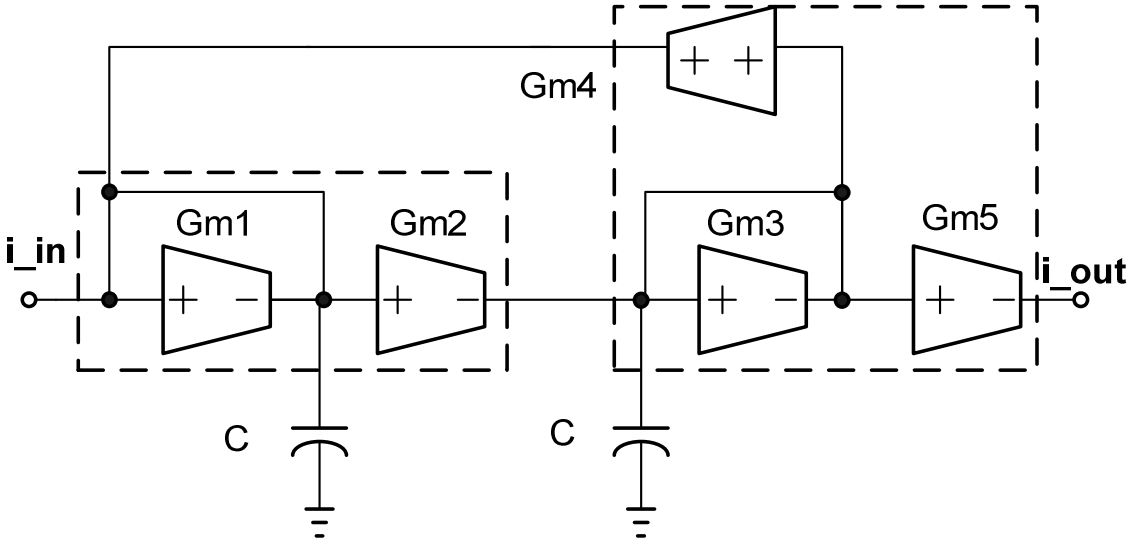


Fig. 3.20 A typical current mode biquadratic section

3.3.2 Current Mode Filters Using the LRCM Structure

Current mode biquadratic filter can be constructed using proposed LRCM structure by noting that the LRCM structure is equivalent to a load transconductor followed by an OTA (Fig. 3.12) and can replace the two OTAs inside the dotted boxes in Fig. 3.20. A fourth current-mode filter is thus designed by cascading two biquads

implemented using proposed LRCM structures. Values of the transconductors are carefully chosen to satisfy Butterworth transfer function and a uniform signal swing across all integrating nodes. Note that since each of the LRCM structures is inverting in nature, transconductor marked Gm4 in Fig. 3.20 would be inverting in actual implementation. This implies that the overall loop thus constructed using LRCM structure would be non-inverting in nature. It is usually not an issue for differential signal paths as the loop can be closed using cross coupled signals from the differential counterpart. However, for practical implementation of the filter common-mode stability needs to be ensured as well.

Positive feedback for common mode signal is not unique to this topology as most biquadratic resonators (voltage mode or current mode) exhibit this property. Use of fully differential transconductor stages (that have appreciable common mode rejection) along with common mode feedback at integrating nodes alleviates the problem by limiting the overall loop gain for common mode signals. However, for pseudo-differential structures like the one proposed, common mode gain of each of the stages is so high (in most instances equivalent to differential signal gain) that the biquadratic loop cannot be stabilized with practical common mode feedback schemes. Past works employing pseudo-differential OTAs or current mirrors have relied on introducing additional common mode losses in all nodes such that the loop gain for common mode signals is less than unity [25],[33]. Losses are introduced by increasing Gm1 and Gm3 significantly while negative impedances (cross coupled load from differential path) are connected to the integrating nodes to compensate for losses for the differential signals.

Significant increase in conductance and the realization of negative impedances introduce circuit noise and increases power consumption. For example, consider the case for a biquadratic section with Q=1.1 (Gm1 = Gm3 = Gm5= 0.5*Gm2 = 0.5*Gm4). Recalling that for proposed LRCM structure (constructed with Gm1 and Gm3), low frequency/DC current gain is given by GM_T/GM_L = Gm2/0.5*Gm1 (a factor of half is result of the fact that at low frequencies only NMOS or PMOS participate as a load conductance to incoming current, ie. GM_L=0.5*Gm1 and GM_T=Gm2). The resultant loop gain for common mode signals can thus be given by: Loop $Gain_{\_CM}$ = $\frac{2*Gm2*2*Gm4}{Gm1*Gm3}$ ~ 16. In order to lower the common mode loop gain to marginally stable value of 1, losses for common mode signals need to be increased by a factor of 4 for each of the integrating nodes. That is $Gm1_{\_CM}$ = 2Gm2 and $Gm3_{\_CM}$ = 2Gm4. This amounts to power increase of almost 75% for the entire biquad.

An alternate strategy is proposed here, wherein an additional mirroring stage is introduced in the feedback. Fig. 3.21 shows the fully differential implementation with the additional mirror stage circled. Parasitic pole of the additional LRCM structure is at frequencies higher than 6GHz. For a power increase of 20% the phase introduced by the additional mirror is minimal to cause any appreciable shift in filter's poles. Since all the integrating nodes are low impedance, common mode levels are self-regulated and dedicated common mode feedbacks are not required.

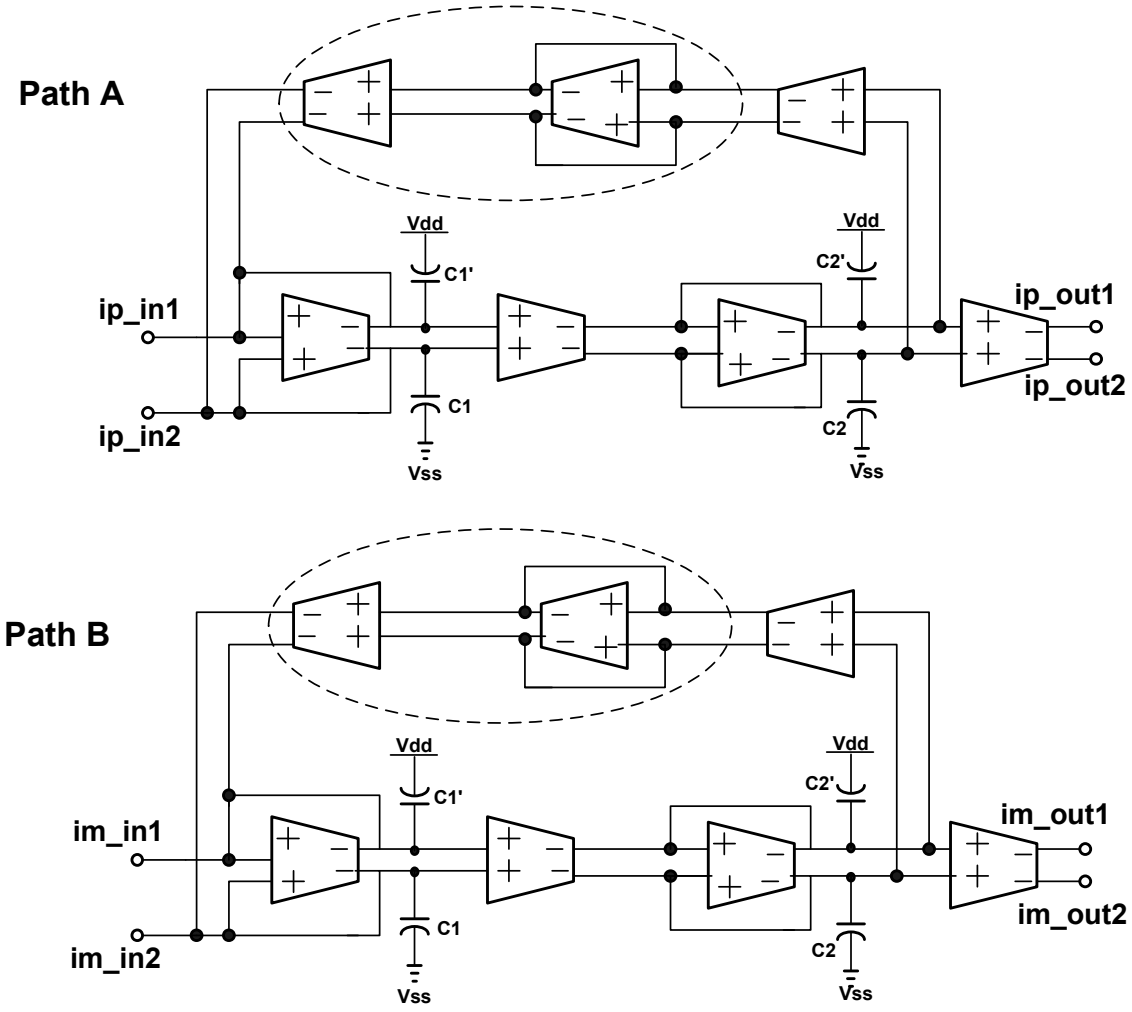


Fig. 3.21 Fully differential biquadratic section realized using LRCM structures

Note that path A in the fully-differential version (Fig. 3.21) is excited through in-phase input currents ip_in1=ip_in2, and path B forms the differential counterpart, excited through another set of in-phase currents im_in1 =im_in2, where im_in1 is out-of-phase from ip_in1. Further, half of the integrating nodes of the dual path structure carry supply/VDD noise (these nodes form the PMOS gates of LRCM structure of Fig.

5) and the other half carry ground/VSS noise (these nodes form the NMOS gates of LRCM structure). Hence, capacitors are connected from each of the integrating nodes to VDD or VSS in accordance to whether these nodes are PMOS or NMOS gates respectively.

3.4 Simulation and Experimental Results

This section discusses simulation and experimental results for the fourth order current mode Butterworth designed by cascading two biquadratic stages realized using LRCM blocks. Simulation results are discussed first followed by the experimental results.

3.4.1 Simulation Results

Fig. 3.22 shows the magnitude plot for the filter. The input is applied as AC current and the output is observed by loading the filter with 50 ohm termination. The filter has -3dB bandwidth of around 1.4GHz and the DC gain (loss) of -1dB.

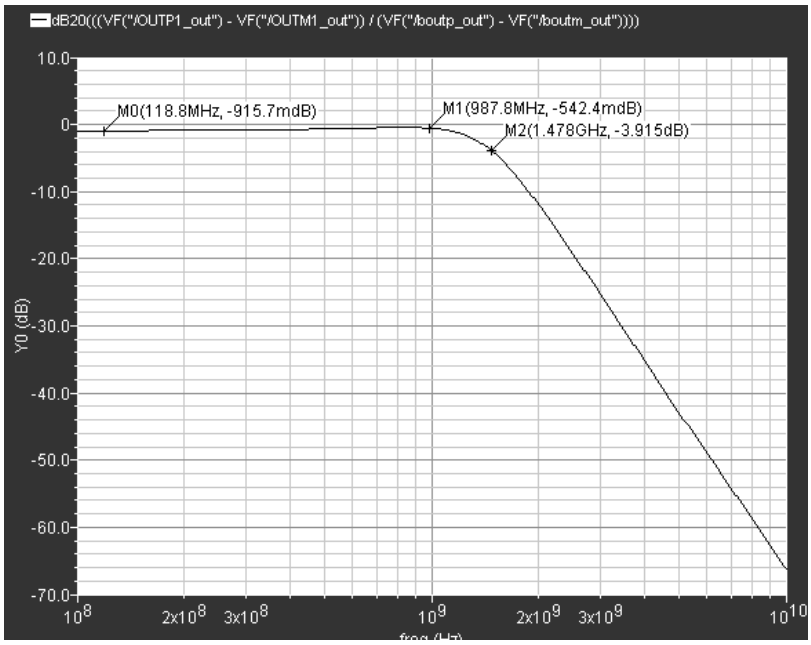


Fig. 3.22 Magnitude response of the fourth order filter based on LRCM structure

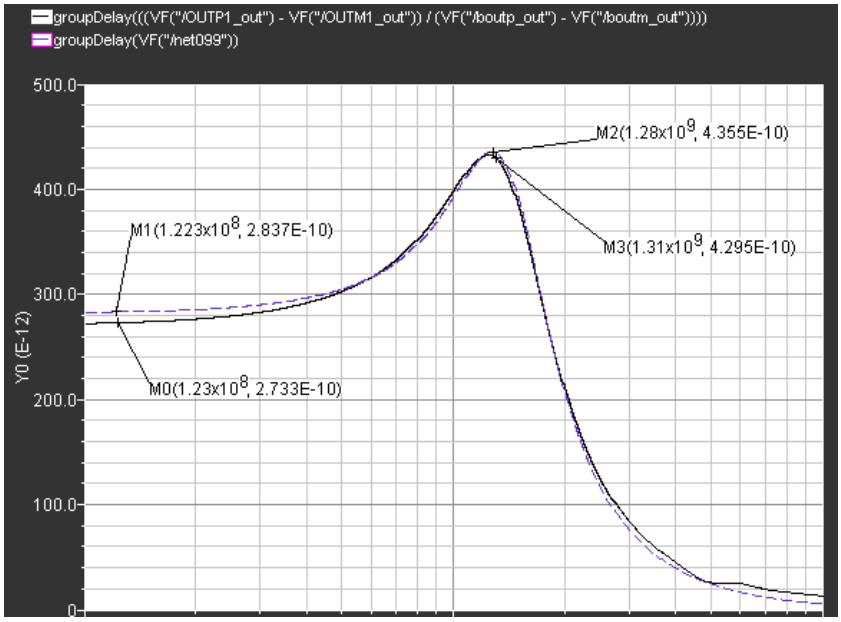


Fig. 3.23 Group delay response of the fourth order filter based on LRCM structure

Fig. 3.23 shows the group delay response of the fourth order LRCM based current mode filter. Also plotted (blue dash) is the response of an ideal forth order Butterworth filter with same resonance frequency. Due to the extra inverting stage in the feedback network, the realized filter is in fact a fifth order system. Hence, it is important to compare these two responses to identify errors because of the additional inverting feedback element. As shown in the figure 3.23, insertion of this additional mirror in the feedback (along with other non idealities) in the system does not change the group delay response appreciably. The low frequency group delay error is 3.5%. The relative group delay error at higher frequencies is progressively smaller except above 6GHz (which is also the frequency of the additional pole in the feedback).

The transient response of the filter is shown in Fig. 3.24-3.25. Fig. 3.24 shows the nominal output current waveform when a 200 MHz input current is injected into the filter. The filter is designed for 700uA p-p differential output signal current.

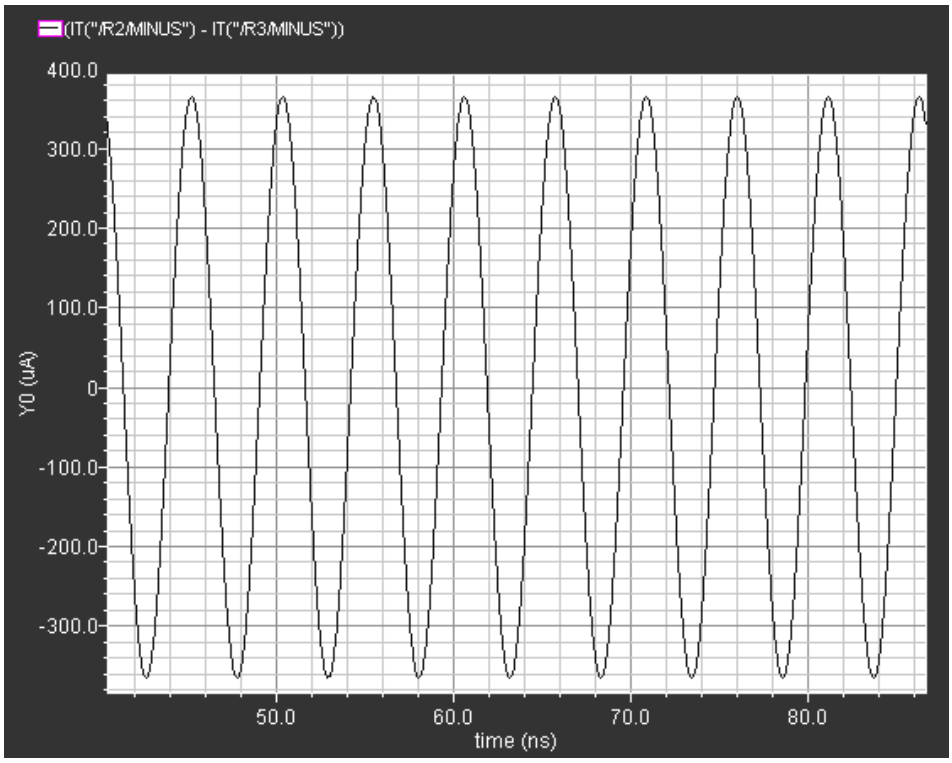


Fig. 3.24 Output current for fourth order current mode filter based on LRCM structure

The input signal current magnitude is adjusted so that internal nodes swing around 250mV p-p differential. For a 1.2 V supply this is a relatively large swing especially for linearity performance better than 50 dB. Fig. 3.25 shows the voltage swing at the first integrating node. The voltage swing at each of the nodes across the filter is roughly 125mV p-p (250 mV p-p differential).

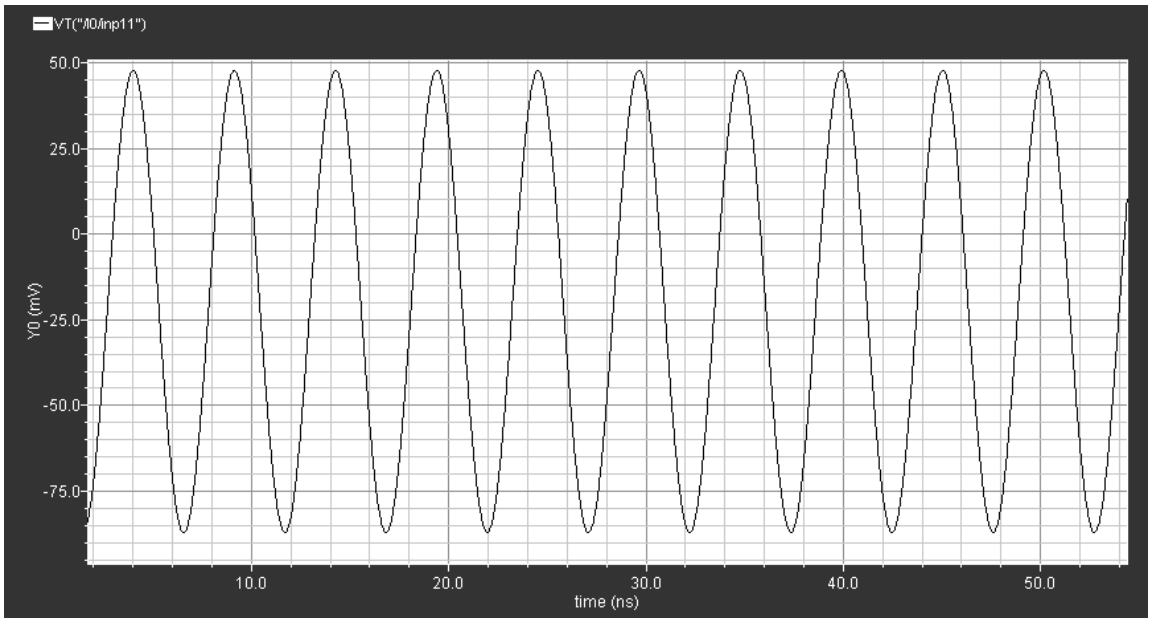


Fig. 3.25 Input voltage swing at the first integrating node

To ascertain the linearity properties of the filter, a 200MHz sinusoid input is applied. The input current magnitude is adjusted so that internal nodes swing to the level of 300mV p-p differential. The observed output spectrum is shown in Fig. 3.26. The plot shows third harmonic distortion of 52.6dB. This is a significant improvement over a simple current mirror or a differential pair. Note that, the improvement in linearity is virtually *free* of noise or power penalty. That is the proposed scheme yields improved linearity without adding any external linearizing element or employing superfluous cancellation schemes.

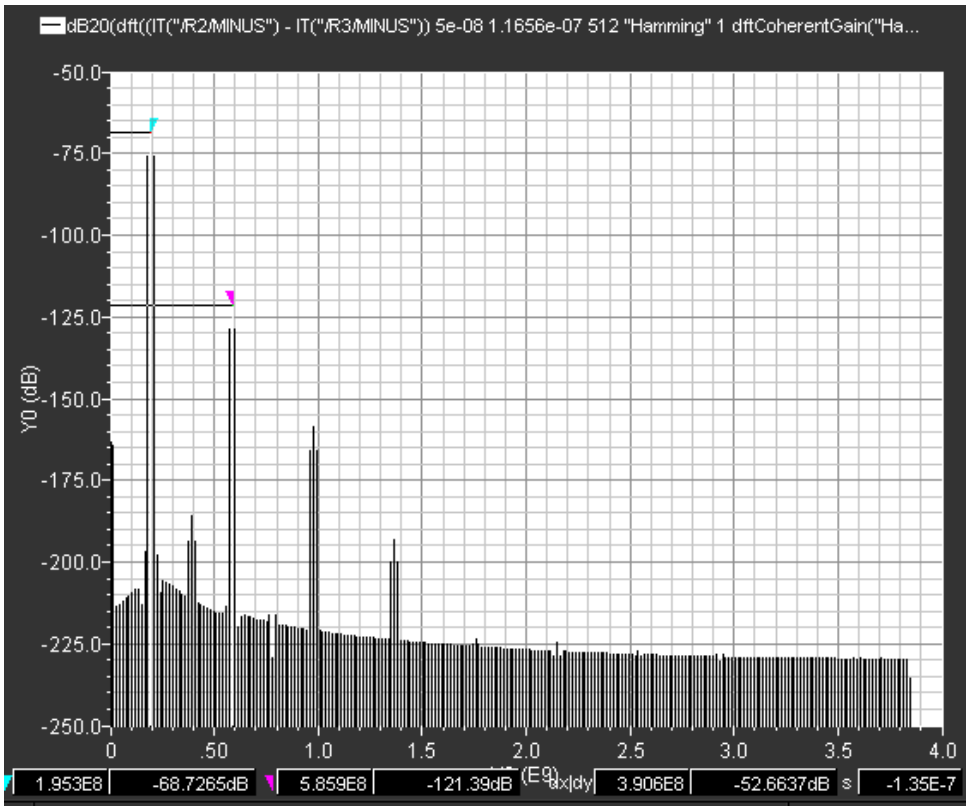


Fig. 3.26 Spectrum of the output current for a 200MHz sinusoid input

To ascertain linearity performance at higher frequencies (around filter's cut-off), a two-tone intermodulation test is carried. Two tones with frequencies around 1GHz (sum of two sinusoids) are applied to the input such that maximum voltage swings are at their nominal values (300mVp-p differential). The output spectrum thus obtained is shown in Fig. 3.27. The third order intermodulation distortion is observed to be around 53dB.

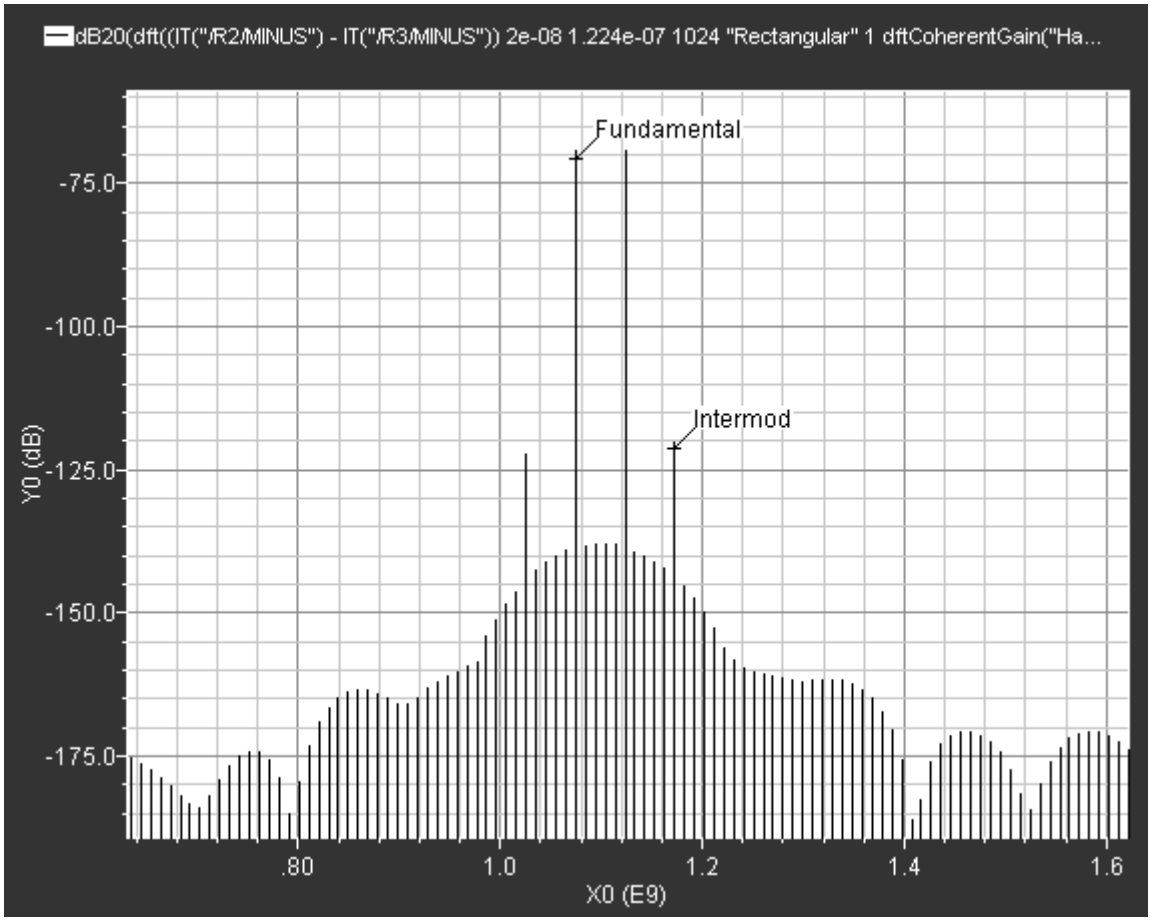


Fig. 3.27 Spectrum of the output current for a two tone inputs

No appreciable degradation of linearity performance is observed as frequency of the input signal is increased from 200MHz to 1GHz. This property is inherent to this structure where improvement in linearity is a result of complementary nature of signal processing and not feedback that may degrade with increased frequencies.

3.4.2 Layout and Experimental Results

A prototype of the proposed filter was fabricated in UMC 0.13µm CMOS technology. Fig. 3.28 shows the layout of the filter and Fig. 3.29 shows the chip micrograph. Since presence of top metal fills hides the details, the layout view is included. The filter occupies silicon area of 0.1mm^2.

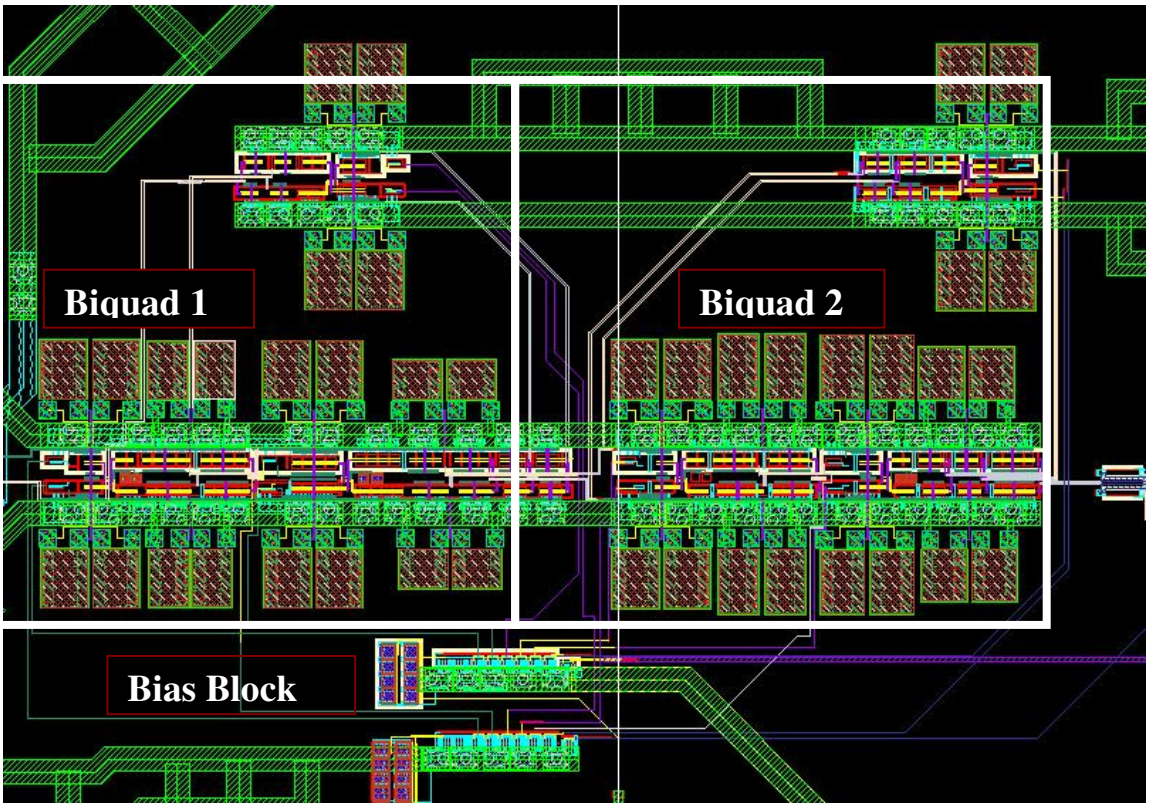


Fig. 3.28 Layout view of the filter

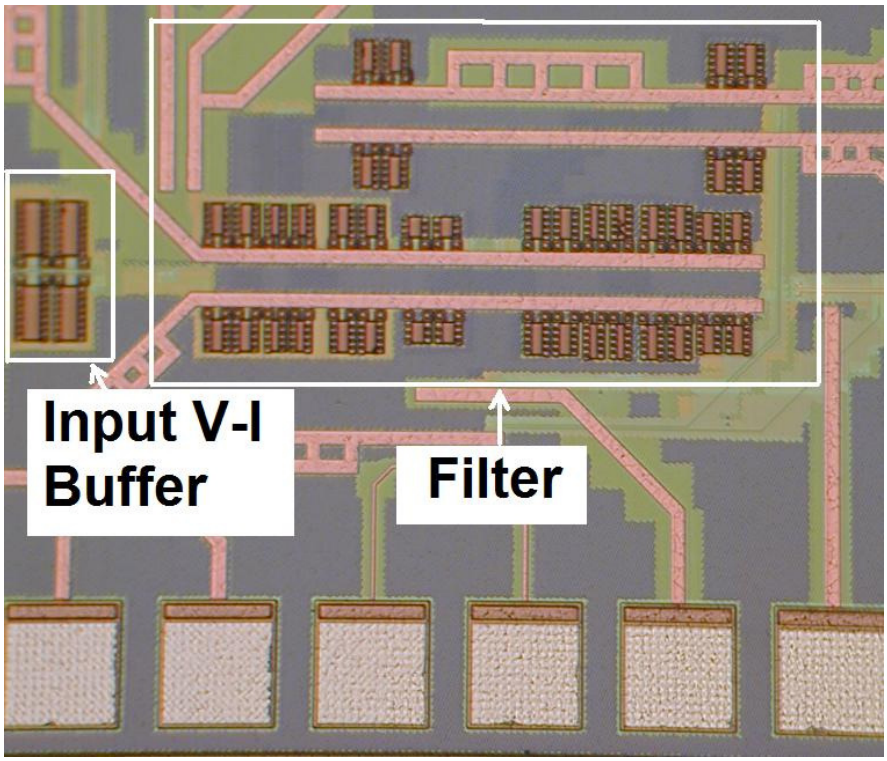


Fig. 3.29 Chip micrograph

Measurement setup is shown in shown in Fig. 3.30. In order to test the current mode filter, input signal current is generated using linear Driver/OTAs. Since the main filter has a total of four current inputs (two pairs of in-phase inputs), a pair of driver OTAs are used for generating differential and copy currents. These OTAs are designed using complementary transconductor operating on a separate supply (VDD_Aux). Separate supplies are used for the main filter and driver OTA so that PSRR measurements can be made without the driver OTA's supply rejection affecting the results. A stand alone Driver/OTA is included to calibrate out losses due to baluns and the driver. Routing to the input and from the output ports to pads is minimized. On chip

poly resistors are used to provide 50 ohm terminations at the input and the output. Such terminations are provided in order to minimize the reflections and to damp the resonant elements: bondwires and capacitors. Fig. 3.31 shows the measurement board.

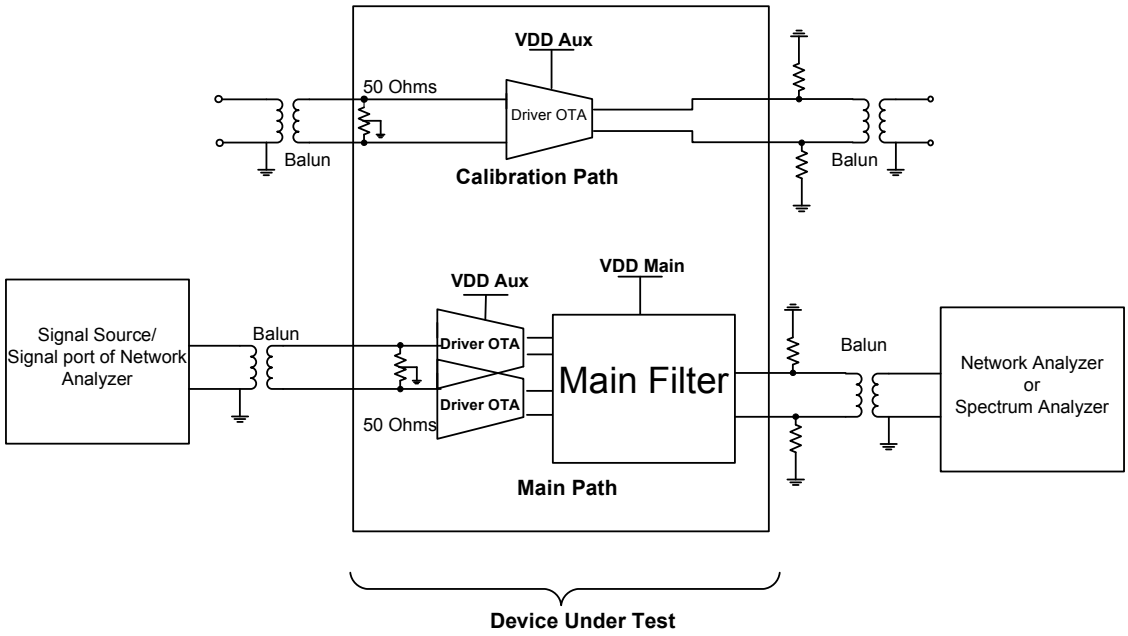


Fig. 3.30 Measurement setup for characterization of the proposed current mode filter

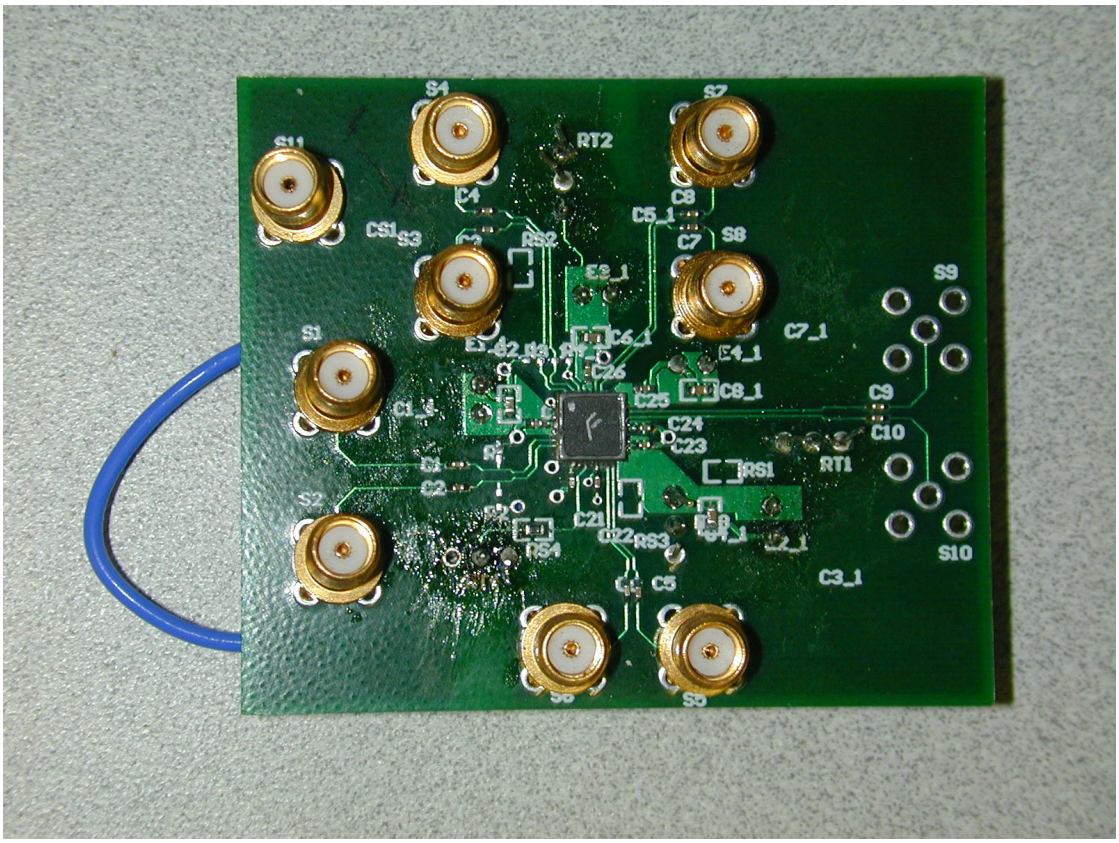


Fig. 3.31 Measurement board

The transfer function of the filter is found by calibrating the filter output with that of a copy V-I buffer. Fig.3.32 shows the measured magnitude response of the filter. The ripple around 1GHz is due to mismatch in the peaking (due to package parasitics) between filter and calibration path. The -3dB bandwidth is observed to be around 1.3GHz.

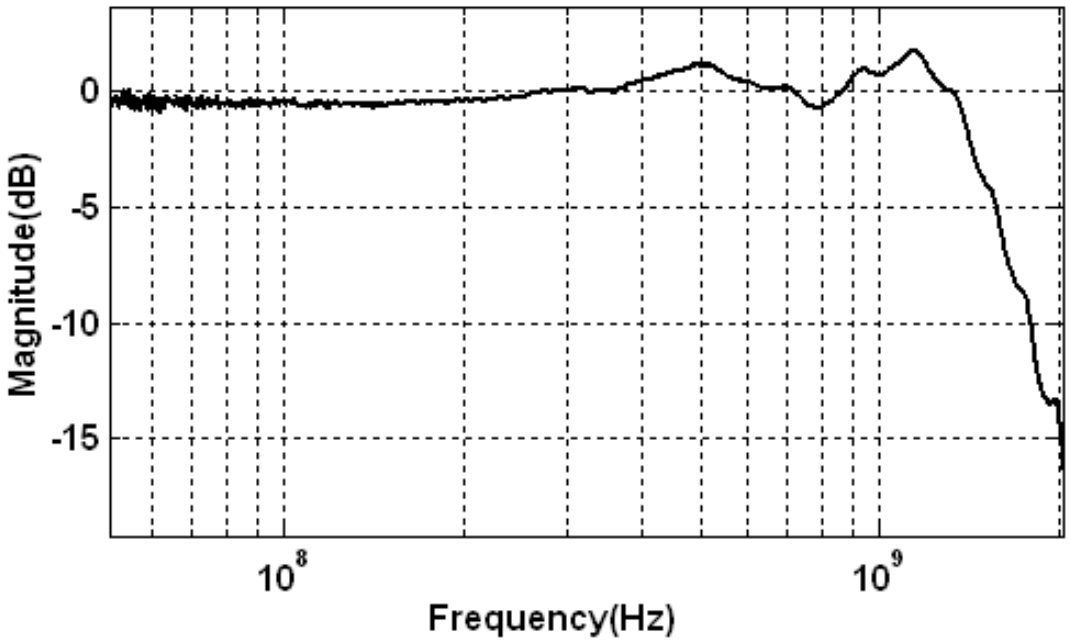


Fig. 3.32 Measured magnitude response

A two tone linearity test is performed with tones applied around 1GHz with 10MHz spacing. The filter shows IM3 of -54.2dB (Fig.3.33). PSSR of the filter (on single-ended output) was measured to be 27dB at 200MHz. Measuring very low signal levels (due to supply noise) at very high frequencies presents difficulties due to ambient RF pick-up. The fourth order filter consumes 24mW of power from a 1.2V supply.

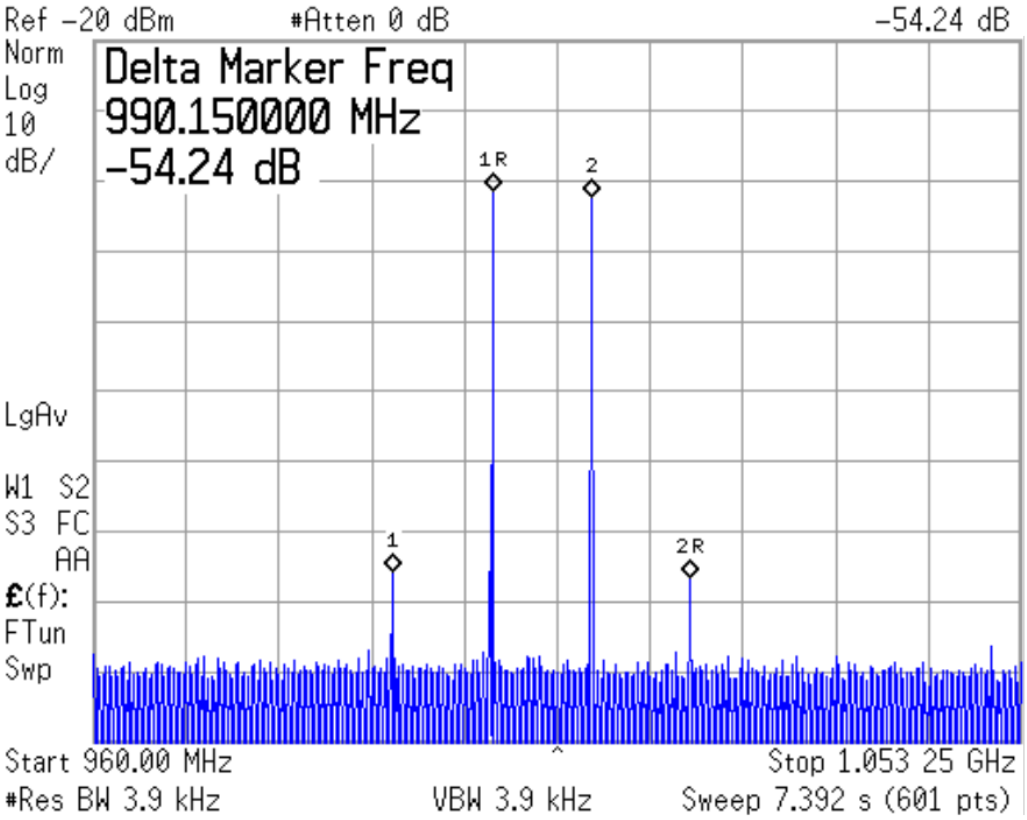


Fig. 3.33 Intermodulation test with input tones around 1GHz

Key performance parameters of the proposed filter and other benchmark Gm-C filters are tabulated in Table.3.2. For comparison a figure of Merit (FOM) is used where FOM = 100*Bandwidth*Order/(Input referred noise*Power).

Table 3.2 Performance summary and comparisons

Reference	[34]	[35]	[36]	This work
Technology (CMOS)	0.35µm	0.18µm	0.13µm	0.13 µm
Supply (V)	3.3	1.5	1.2	1.2
Filter Order	5	4	5	4
Bandwidth (MHz)	500	1000	240	1300
Noise (µVrms)	366	1389	117	266
Linearity	THD=-40dB at 0.5Vpp	IM3=-43dB at 0.35Vpp	OIP3= -18dBV	IM3=-54dB at 0.3Vpp
Power (mW)	100	175*	24	24
FOM	6.83	1.64	42.7	81.45

* Includes automatic tuning

3.5 Conclusions

A highly power-efficient and linear dual-path current-mirror based element is presented. A fourth order Butterworth filter with bandwidth of 1.3GHz is implemented using the proposed element. The filter, thus designed, is found to have best power efficiency amongst the similar class of filters. The power efficiency of the filter is a direct result of a highly linear and power-efficient (low noise for given power) complementary current mirroring block that processes signal through complementary signal paths and results in efficiency improvement of nearly seven times.

This class of filters can find applicability in wideband filtering (few hundreds of MHz to GHz range) such as disk drive channels and high data rate communication. Significant power gains can be achieved by use of proposed LRCM structure for such filters. Scalability of the proposed LRCM structure with technology makes it a suitable candidate for filters integrated in futuristic digital CMOS technologies.

The presented filter is a proof-of-concept that shows the implementation of a current mode filter using the proposed efficient complementary mirroring structure. Additional features such as equalization gain can be implemented using techniques and architectures discussed in the previous chapter. Future scope of work may also include investigations regarding optimum programmability and tuning mechanism. Filter programmability can be achieved by either tuning the bias voltages that determine the DC current or by switching the mirror cells.

CHAPTER IV

A 68DB SNDR ACTIVE RC FILTER FOR 10 BIT CONTINUOUS-TIME DELTA-SIGMA ADC

4.1 Introduction

Real world signals are generally expressed as continuum of values. Such analog signals are processed through a signal processing chain before being applied to a traditional digital computing core. Core function of such signal processing chain is to digitize the analog signals with least possible noise and power overhead. Sampling is a necessary step to be carried for converting an analog signal to a digital stream. Sampling is almost always preceded by band-limiting filters to prevent aliasing. Fig. 4.1 shows a typical analog chain consisting of analog pre-processing, anti-aliasing filter and an Analog to Digital Converter (ADC).

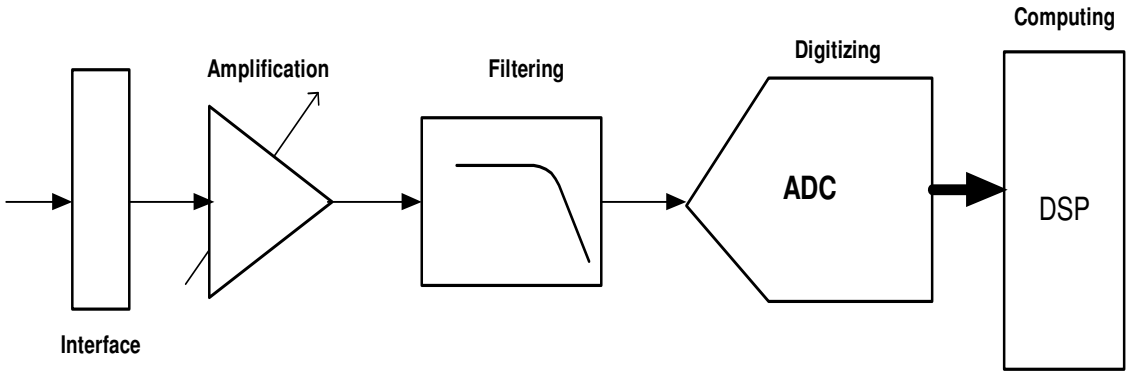


Fig. 4.1 A typical analog chain digitizing real world signals

There are at least two points in this chain where a filtering function may be required: a) prior to the ADC as an anti alias filter. b) as a filter inside the core ADC for certain architectures (delta-sigma). In this chapter we concentrate on filter design for a particular delta-sigma ADC.

Delta-Sigma Modulators have gained popularity in medium to high resolution space due to their amenability to scaled digital technologies. Generalized delta sigma architecture is shown in Fig. 4.2. For typical single-bit architectures, the quantizer and the filter are the only essential analog blocks while much of the processing is performed by a back end digital (DSP). Noise shaping and extensive digital filtering allows use of a relatively coarse quantizer.

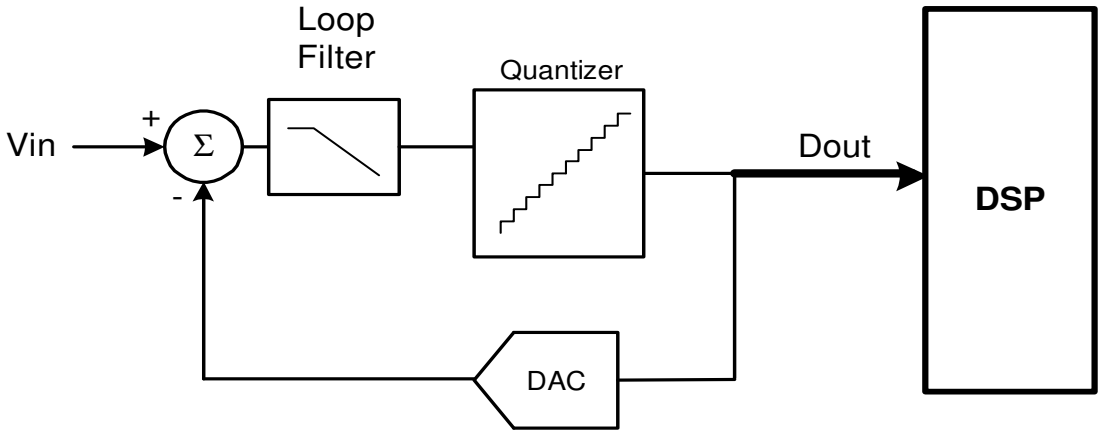


Fig. 4.2 A typical delta-sigma based analog to digital converter

The primary focus of this design has been a filter for a WLAN analog to digital converter. Sigma delta ADC architectures have dominated the space for wireless

applications [37-39], with signal bandwidth in MHz range and resolution around 10-11 bits. With popularity of smart-phones and hand held multimedia devices, an impressive array of features are being offered on single wireless device. These ICs offer high level of integration while utilizing a very small footprint. This rapid integration and system miniaturization has given way to the trends of shifting most of the signal processing functions to the digital part of IC. This has also resulted in emergence of new philosophies and directions in signal processing [40].

4.1.1 A Novel ADC Architecture

Motivated by the principle of digital-centric design, a novel architecture for a delta sigma based ADC is proposed [41]. The architecture leverages the strength of digital CMOS scaling by converting traditional analog blocks to digital implementation and voltage represented signal to time edge representation. Fig. 4.3 shows a simplified block diagram for this continuous time delta sigma ADC. Following the filtering, signal is sampled and converted to a pulsed waveform whose width is proportional to sampled signal voltage. Pulse Width Modulator (PWM) generator is used to this effect. Finally, a Time to Digital Converter quantizes the time represented pulse to discrete edges. It generates a digital code representing the rising and falling edge as well as a time quantized pulse waveform that is fed back to the filter. Note that TDC functions in lieu of a traditional quantizer. It also generates the feedback pulse that realizes an equivalent to multilevel DAC feedback.

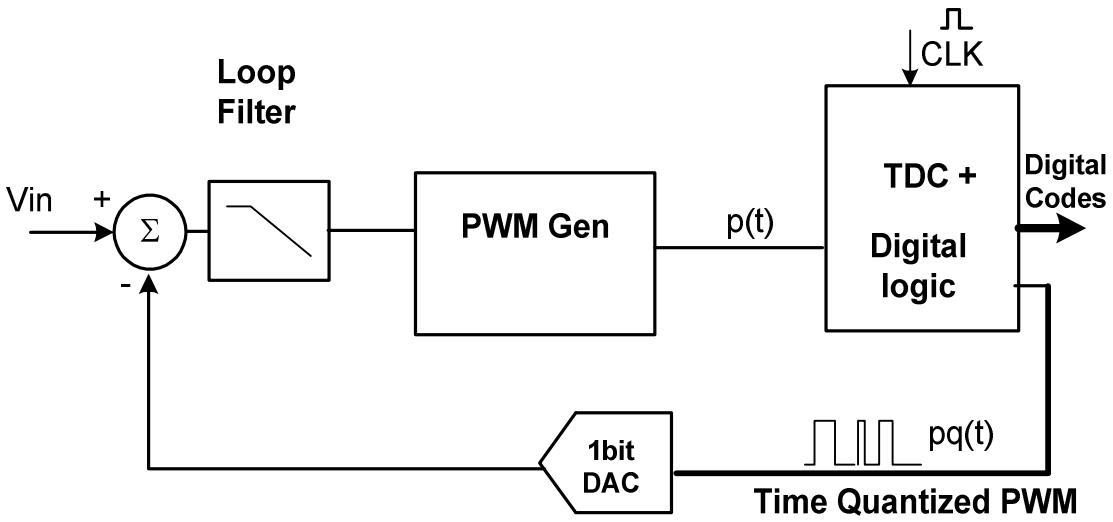


Fig. 4.3 A novel continuous time delta sigma and TDC based ADC architecture

4.1.2 Filter Design Challenges

Filter design for the proposed ADC presents many challenges in terms of architecture, use of technology and above all integration in a hitherto unknown system. The proposed WLAN ADC is targeted for 10 bits resolution in 20MHz of signal bandwidth. Hence, the dynamic range of the designed filter should be equivalent to 11-12 bits, so that it does not limit the overall performance. Other sets of challenges arise from the choice of technology. Since the performance of the architecture can best be proven and utilized for fine-line digital CMOS technology, TI 65nm CMOS is the technology of choice for design and fabrication. Realizing performance and robustness of analog design for such deep submicron technology presents its unique challenges [42]. Lastly, since this filter is a part of a recently proposed and, at the time, unproven

system, interface with adjoining blocks such as PWM sampler, TDC-DAC needs to be handled carefully and warrant thorough simulations to uncover unexpected issues.

4.2 Filter Design for 20 MHz, 68dB Continuous-Time Delta-Sigma

4.2.1 Transfer Function of the Loop Filter

This section pertains to the system design of filter for the above mentioned continuous-time delta-sigma ADC. System design, here, refers to the design and choice of noise transfer function and the corresponding filtering function for an optimized performance. The most common noise transfer function for nth order filtering is given (z domain) as:

$$\text{NTF1} = (1 - z^{-1})^{n} \tag{4.1}$$

This generalized noise transfer function places all poles at DC (z=1) and an equal number of zeros at z=0. Idealized gain of the NTF1 at DC is 0. However, non idealities such has finite integrator gain and other noise sources (thermal and flicker) limit the low frequency noise floor.

Alternately, zeros can be spread in signal bandwidth to give flatter in-band noise characteristics [43]. This approach optimizes the SQNR while pushing out the zeros to higher frequencies. Note that, with the spreading of zeros ‘out of band’ gain of the noise transfer function may increase with cost to stability; unless pole locations are re-optimized.

Through system simulations, a third order filtering (chosen clock frequency of 250MHz and 50 quantization levels in time) is found to be sufficient to achieve the required performance [41]. For this design, a third order inverse Chebyshef highpass type function is chosen as the noise transfer function. This particular filtering function is chosen empirically on the basis of the fact that a highpass inverse Chebyshef would entail a roughly equiripple in-band noise characteristics. An ideal inverse Chebyshef highpass function maintains the signal-band ripple to a certain maximum value; it also has infinite quality-factor poles spread over the signal bandwidth. For practical realization, the quality factor of the poles has been limited to 8. The equivalent noise transfer function is plotted in Fig. 4.4.

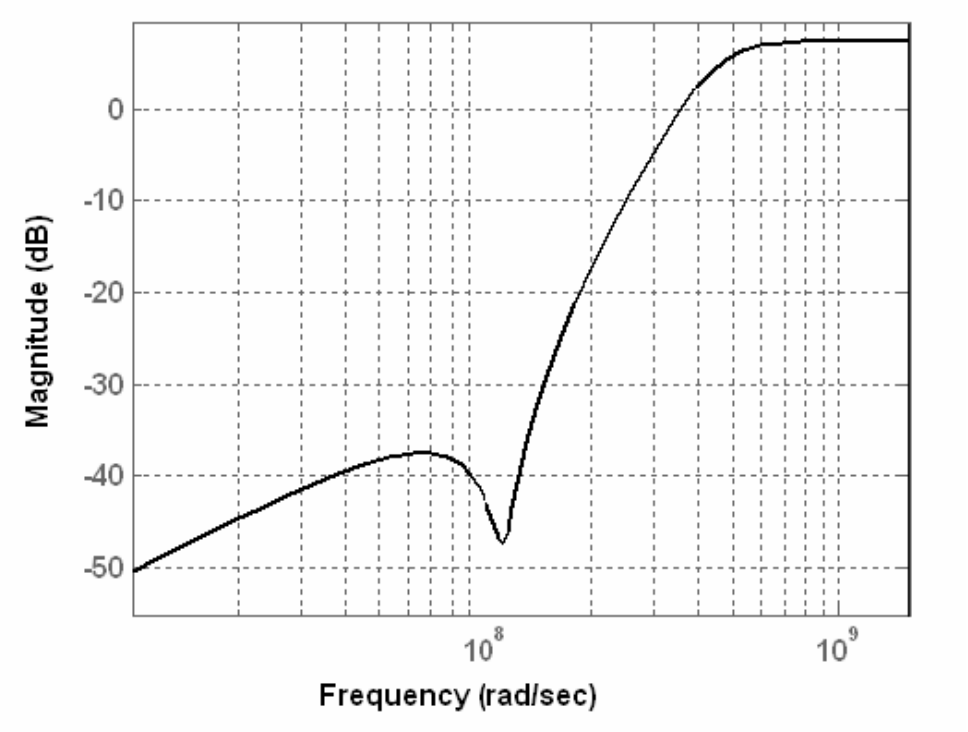


Fig. 4.4 Ideal noise transfer function

Transfer function of the corresponding loop filter is given by:

$$H(z) = \frac{1.622z^2 - 2.093z + 0.8024}{z^3 - 2.922z^2 + 2.894z - 0.9721} \tag{4.2}$$

Equivalent continuous time filter is derived using MATLAB toolbox with sampling frequency of 500MHz. The corresponding continuous time transfer function is given by:

$$H(s) = \frac{5.908e8s^2 + 2.086e17s + 4.223e25}{s(s^2 + 1.414e7s + 1.279e16)} \tag{4.3}$$

The above transfer function has a pair of complex poles located at fo = 18.5MHz and Q_P of 8 and an integrating pole located at DC. The complex zeros for this filter are at fz = 52.4MHz with Q_Z = 0.2.

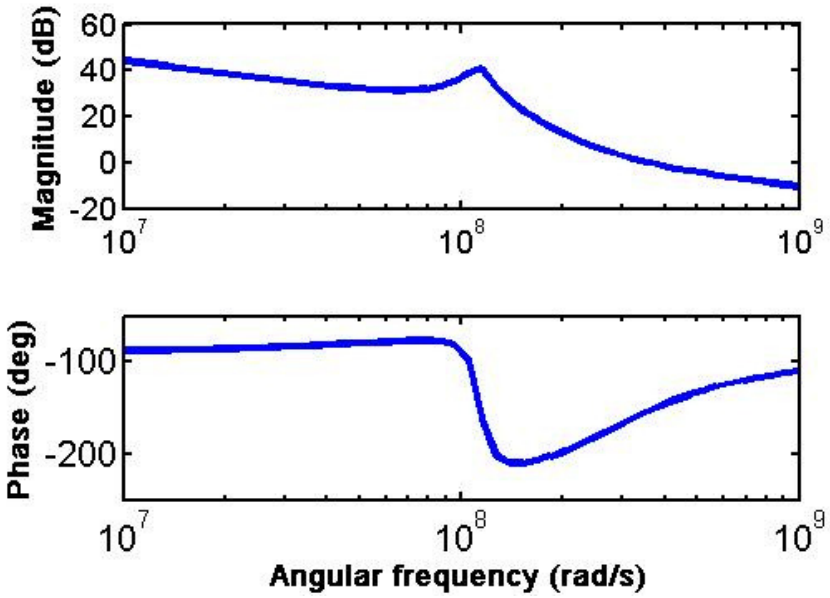


Fig. 4.5 Magnitude and phase response of the ideal filter

The magnitude plot of the ideal filter is shown in Fig. 4.5. Note that, the low frequency (DC) gain of the filter is 42dB, while the minimum in-band gain is kept at 37dB. DC gain of the filter is an important quantity in terms of implementation, as would be seen in later parts of this chapter. The minimum in band gain dictates how much suppression filter offers to the non-idealities (and noise) of the subsequent blocks and stages.

4.2.2 Specifications of the Loop Filter

Loop filter provides necessary filtering (shaping) to the quantization noise. Determination of the order and the type of filter was done using system considerations discussed in detail in previous section.

Next, noise and distortion specifications are determined on the basis of required dynamic range of delta-sigma converter. For the 10 effective numbers of bits of the analog to digital converter, 62dB of noise (quantization and device) and distortion is budgeted from all sources. Half of this power is budgeted for non linearity due to non uniform timing steps of TDC [41]. This brings specified device and quantization noise along with distortion from other sources to 65dB. Since device (thermal component) of noise trades directly with power, it is customary for an efficient design to be limited by device noise and distortion (and not by quantization noise). Half of the above noise and distortion power is budgeted for filter and rest half for other components (DAC, PWM and TDC). This brings Filter's SNDR specifications to 68dB.

4.3 Implementation Details

4.3.1 System Design Considerations

The third order filter, to be designed, needs to implement a pair of complex poles and a real integrating pole (at DC) besides a pair of complex zeros. Thus, the filter implementation in general would consist of a biquadratic section that realizes complex poles and an integrator. It is important to mention here that the choice of filter implementation is limited to active RC one because of high dynamic range (68dB) requirement albeit with relatively moderate bandwidth (20MHz). For optimum ordering of the two sections (biquad and integrator), the following considerations are taken into account:

a) The initial section should provide sufficient gain for suppressing noise (thermal and flicker) of the subsequent stages. Thus if the biquadratic section precedes the integrator, sufficient low frequency gain should be built into it. This consideration would be discussed further, later in this chapter.

b) Complex zeros can be readily implemented if the biquadratic section precedes the integrating section. Bandpass and lowpass functions generated through the biquadratic section can be summed through the virtual ground of the following integrator to yield a pair of complex zeros.

Thus, the chosen filter architecture consists of a biquadratic section followed by a lossless integrator. Fig. 4.6 shows the block diagram and the corresponding active RC realization. R1-C1-R_Q-Amp1, R2-C2-Amp2 along with R_F realize the biquadratic

resonator. Lowpass signal is tapped from V_lp node while bandpass function is available at V_bp. R3-C3 along with Amp3 realize a lossless integrator.

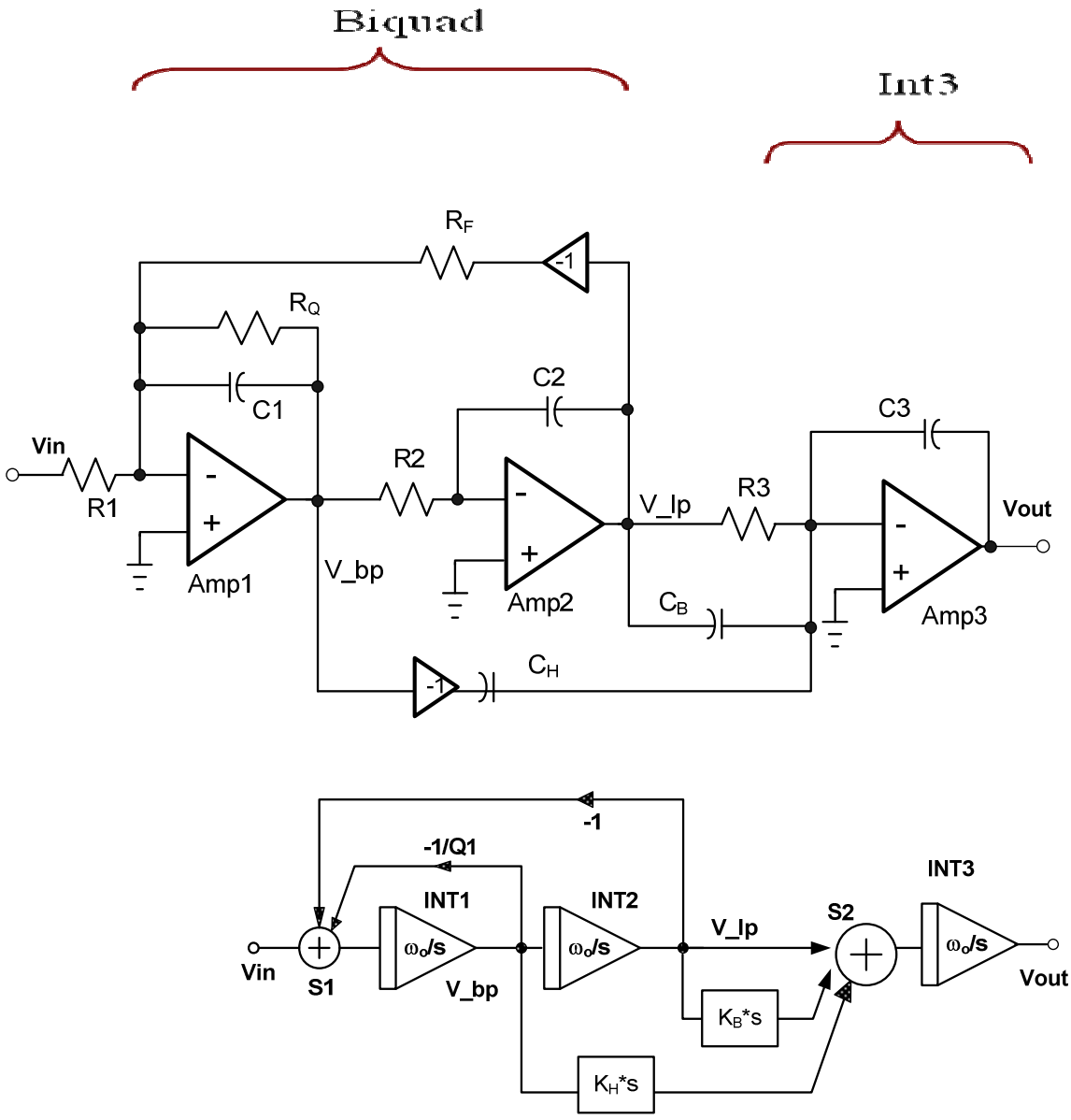


Fig. 4.6 Third order filter architecture with a pair of complex zeros

For compact implementation, complex zeros are realized by summing up appropriate signals at the virtual ground of the last integrator. Thus lowpass and bandpass signals are capacitively coupled to integrator 3 to yield bandpass and highpass signals at the filter output. The addition of the third-order filtering and second-order lowpass and second-order bandpass function yields a pair of well defined complex zero along with the desired third order filtering function as given by 4.4:

$$H(s) = \frac{Vout(s)}{Vin(s)} = \left(\frac{\frac{\omega_o^2}{\omega_Z^2}(s^2 + \frac{\omega_z}{Qz} * s + \omega_z^2)}{s^2 + \frac{\omega_o}{Q_P} * s + \omega_o^2} \right) * \left(\frac{\omega_I}{s} \right) \tag{4.4}$$

$$\omega_o = \sqrt{\frac{1}{R_F * R2 * C1 * C2}}$$

$$\omega_Z = \sqrt{\frac{1}{R3 * R2 * C_H * C2}}$$

$$Q_P = \sqrt{\frac{C1 * R_Q^2}{R_F * R2 ** C2}}$$

$$Q_z = \sqrt{\frac{R2 * C_H * C2}{R3 * C_B^2}}$$

$$\omega_I = \frac{R_F}{R1 * R3 * C3} \tag{4.5}$$

In the actual implementation, each of the resistors and capacitors of Fig. 4.6 is realized using a bank of components controlled through series switches. These switches are strategically placed at the low swing nodes (for example virtual ground of the amplifier) so that linearity of the switches does not limit the system performance. Thus, integrator time constants and zero locations are digitally programmable over the expected process and temperature variations.

4.3.2 Component Design Considerations

Noise Considerations: As discussed in the previous sections, stated requirement of the designed filter is to have SNDR better than 70dB. With the reasonable assumption that noise limits SNDR (active RC filters can be designed with excellent linearity performance); for 1.08V ADC reference and -5dBFs input signal, input referred noise specifications for the filter can be derived to be 67.8 μV rms. The noise is budgeted into various components (resistors and amplifiers) in order to derive component values and amplifier specifications.

Noise from input resistor R1 and Amp1 directly appears at the input of the filter while noise from each of the integrator 2 and integrator 3 is attenuated by gain of the preceding stages. Ignoring C_H and C_B coupling paths, the expression for the input referred rms noise is given by:

$$\text{Vrms} = \sqrt{\text{Vn}_{\text{R1}}^2 + \text{Vn}_{\text{amp1}}^2 + \left(\frac{\text{R1}}{\text{R}_\text{F}}\right)^2 * \text{Vn}_{\text{RF}}^2 + \left(\frac{1}{\text{TF}_{\text{int1}}}\right)^2 * \text{Vn}_{\text{INT2}}^2 + \left(\frac{1}{\text{TF}_{\text{biquad}}}\right)^2 * \text{Vn}_{\text{INT3}}^2} \quad (4.6)$$

where Vn_{R1}^2 is the input referred integrated noise power due to resistor R1, Vn_{amp1}^2 is input referred noise power due to Amp1 and so on. TF_{int1} corresponds to the gain transfer function of integrator 1 and TF_{biquad} refers to gain transfer function of the biquad. The overall noise of the filter can be designed to be limited by the input resistor (R1) and the first opamp (Amp1). With pragmatic design techniques it can be ensured that noise of feedback resistor and integrator 2 and 3 have negligible contributions to the total noise. Making an initial assumption of equal noise contribution from R1 and Amp1, and these two being the only dominant noise sources, the value of resistor R1 is determined to be 3K.

Another consideration to be taken into account is gain distribution. A direct implementation of (4.3) would entail a unity gain (low frequency gain~1) biquadratic filter followed by an integrator with 550MHz gain-bandwidth. The integrator 1 and integrator 2 would, in this case, have gain-bandwidth to be equal to resonance frequency of 18.5 MHz. However, it is preferable to embed a significant part of low frequency gain in the biquad (distributed over integrator 1 and integrator 2). Specifically, in this case a gain of 4 is built into integrator 1 and a gain of 2 is built into integrator 2 such that the overall biquad has a low frequency gain of 8. This not only results in a simplified component design but also yields a design optimized for noise and power as per the reasons outlined below:

a) Gain at the initial stages attenuates noise of the later integrators when referred at the input. For example, noise from R2 and Amp2 would be lowered by a factor of 16 (at ωo) when referred to the input of the filter.

b) Process of embedding gain in the biquad, yields a more practical choice of component values. For example, for resonance frequency of 18.5MHz, integrating capacitor C1 would be 2.8pF as input resistor R1 is 3K. However with a gain of 4 built into integrator 1, C1 can be scaled down by a factor of 4. Similarly C2 can be scaled down by a factor of 2 and Rf scaled up by a factor of 8. Table 4.1 shows the value of key components before and after scaling.

Table 4.1 Filter scaling

Biquad Gain	Int1 gain-bandwidth	Int2 gain-bandwidth	Int3 gain-bandwidth	R1/C1	R2/C2	R3/C3	R_F
				Actual component values (includes parasitic effects)			
1	18.5MHz	18.5MHz	550MHz	3K/ 2.8pF	6K/ 1.2pF	1K/ 320f	3K
8	72MHz	36MHz	68MHz	3K/ 620fF	6K/ 600fF	8K/ 320f	24K

c) Another advantage of such scaling is the reduced spread in the gain bandwidth of integrators. This results on more uniform design and layout and saving in terms of time.

d) Finally, since R_F is scaled up by a factor of 8, its noise contribution is diminished by a factor of 8 as per 4.6.

To summarize the noise benefit associated with scaling, equation 4.6 is rewritten for the two cases as following:

Original (un-scaled version):

$$Vrms = \sqrt{Vn_{R1}^2 + Vn_{amp1}^2 + \frac{4KTR1^2}{Rf} + \left(\frac{1}{TF_{int1}}\right)^2 * Vn_{INT2}^2 + \left(\frac{1}{TF_{biquad}}\right)^2 * Vn_{INT3}^2} \quad (4.7a)$$

After scaling, R_F_scaled =8 R_F, TF_{int1}_scaled = 4*TF_{int1} and TF_{biquad}_scaled = 8*TF_{biquad}

$$Vrms' = \sqrt{Vn_{R1}^2 + Vn_{amp1}^2 + \frac{4KTR1^2}{8*R_F} + \left(\frac{1}{4*TF_{int1}}\right)^2 * Vn_{INT2}^2 + \left(\frac{1}{8*TF_{biquad}}\right)^2 * Vn_{INT3}^2} \quad (4.7b)$$

Thus, through effective gain distribution and scaling of components, it is ensured that R1 and Amp1 are the main contributors of noise in the filter.

4.4 Design of Integrators

4.4.1 Integrator 1 and Integrator 2 Design

Integrator specifications and component values were derived in the previous section on the basis of noise and system specifications. These form the basis for the corresponding amplifier specifications. In order to have sufficient loop gain at integrating bandwidth, gain-bandwidth for the amplifiers is chosen to be 3-4 times the integrator gain-bandwidth-product. Gain-bandwidth of the amplifier refers to product of low frequency gain and the dominant pole for amplifier configured in ‘open-loop’ mode

(ie. feedback is not closed through RC) Table 4.2 summarizes integrator 1 and integrator 2 specifications along with the corresponding swing requirements.

Table 4.2 Integrator 1 and integrator 2 gain-bandwidth and swing specifications

Integrator 1	**Integrator 2**
Integrator Gain-Bandwidth: 72MHz	Integrator Gain-Bandwidth: 36MHz
Amplifier Gain-Bandwidth> 250MHz	Amplifier Gain-Bandwidth> 140MHz
Output Swing: 400mV p-p Differential	Output Swing: 200mV p-p Differential

Note that, since integrator 1 also propagates unfiltered quantization noise (through DAC path), its output experiences a higher transient swing: 400mV p-p differential. Other requirements for the two amplifiers included a reasonable phase (>60Degree) and Gain (>10dB) margins. It is important to mention that though a phase margin of 60Degree or better would in general suffice for a continuous time amplifying block, efforts should be made to have minimum possible excess phase. An excess phase translates directly to loop delay and may easily de-stabilize a continuous time delta-sigma loop.

A simple two stage amplifier: A PMOS differential pair followed by Class-A NMOS driver is chosen for integrator 1 and integrator 2. Following reasons outline the choice of such architecture:

a) Each of the two integrators is required to have a minimum DC gain requirement of around 30dB. The specifications are derived using an extensive

MATLAB model outlined in [41]. In order to meet this requirement in deep submicron technologies such as the 65nm CMOS, two stages of amplifications are necessary.

b) For the given deep submicron technology, flicker noise corner for minimum size devices is beyond 1GHz. Since stringent noise specifications need to account for the in-band flicker noise, PMOS devices are used as input drivers to minimize flicker noise contribution.

c) Use of two stage amplifier also decouples the output load from the input stage specifications. For example, the input stage can be independently sized to meet thermal and flicker noise requirement, while the output stage is sized to drive the load from the later stages. Gain-bandwidth of the amplifier can also be independently determined through compensation capacitor.

d) Finally a fully differential pair is used as the input stage. Biasing the transistors for a fully differential stage (with tail current) is a little challenging for a 1.2V design. But, a pseudo differential stage is avoided as any supply noise injected so early in the filtering chain would appear directly at the input of the filter.

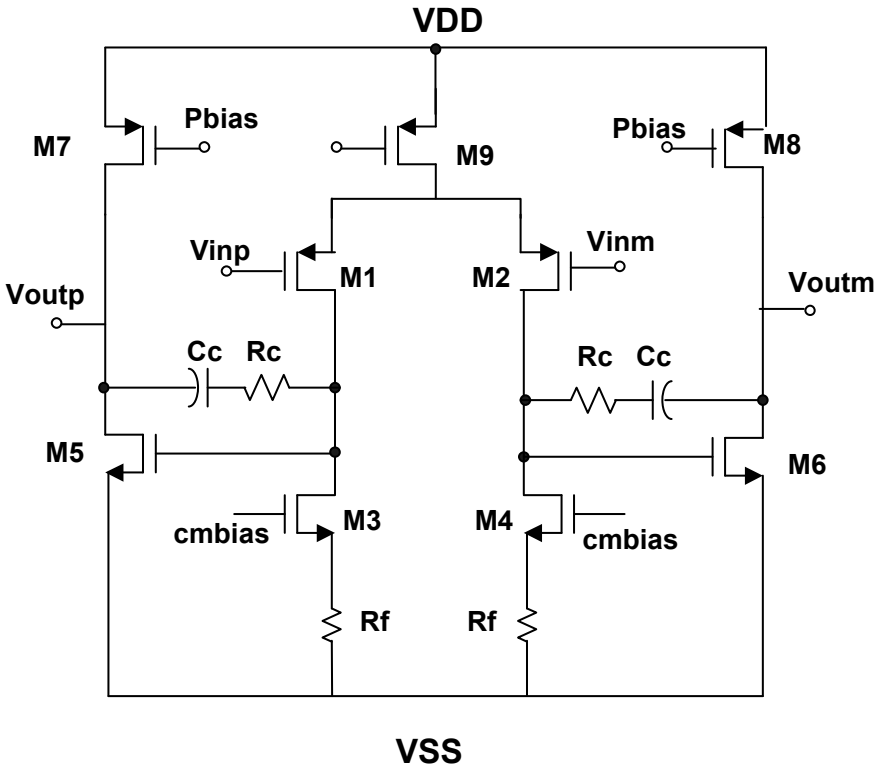


Fig. 4.7 Schematic: amplifier 1 and amplifier 2

Fig. 4.7 shows the schematic for amplifier 1 and amplifier 2. M1, M2 and M9 form the PMOS differential pair. M3 and M4 are the NMOS current sources that are controlled through a dedicated common mode feedback loop. It will be shown that resistors Rf serve an important function by degenerating NMOS current sources. M5 and M6 are output drivers while M7 and M8 form the PMOS current sources. Note that M1, M3, M9 along with Rf need to be biased in the available supply of 0-1.2. Hence, input common mode of 450mV is chosen for the PMOS drivers. This is 150mV below the half supply threshold (supply levels are 1.2V and 0V).

Noise of input drivers M1 and M2 can directly be reflected at the input port, while noise of current source M9 would appear as a common mode signal. Noise from the output devices M5-M8 would be attenuated through the first stage gain when viewed at the amplifier input. Transistors M1 and M2 are the dominant noise sources. They are biased and sized such that thermal and flicker noise are under specified limits. As discussed earlier flicker noise is one of the limiting design parameters. In order to reduce the flicker noise contribution from M3-M4, degeneration resistor Rf is introduced. Rf is realized using poly resistors and is sized to have negligible contribution to flicker noise. While the introduction of Rf reduces the current noise contributed through M3 and M4 by a factor of $\eta = (1+gm*Rf)^2$; it reduces the available headroom for biasing M3-M4 by voltage drop across Rf. For this design, the maximum allowable value of Rf is chosen such that voltage drop across the resistor does not exceed 100mV. Table 4.3 shows the sizes of the devices for amplifier 1 and amplifier 2.

Table 4.3 Device sizes for amplifier 1 and amplifier 2

	M1-M2	**M3-M4**	**Rf**	**M5-M6**	**Rc/ Cc**	**Idc**
Amplifier 1	8(11/0.4)	4(5/1)	1K	16(1.3/0.13)	2K/700f	1.9mA
Amplifier 2	8(2.7/0.4)	4(3/1)	3K	14(1.5/0.13)	2.4K/450f	1.1mA

A common mode control loop is added around each of the amplifiers to stabilize the output common mode to the desired value. In case of Amplifier 1, output common mode is held at 0.45V while for amplifier 2 it is stabilized at 0.6V. The common mode is detected using a center tapped resistor-capacitor network and is then applied to an error amplifier which compares it to the predefined reference. Fig. 4.8 shows the common mode control setup for the amplifier in Fig. 4.7.

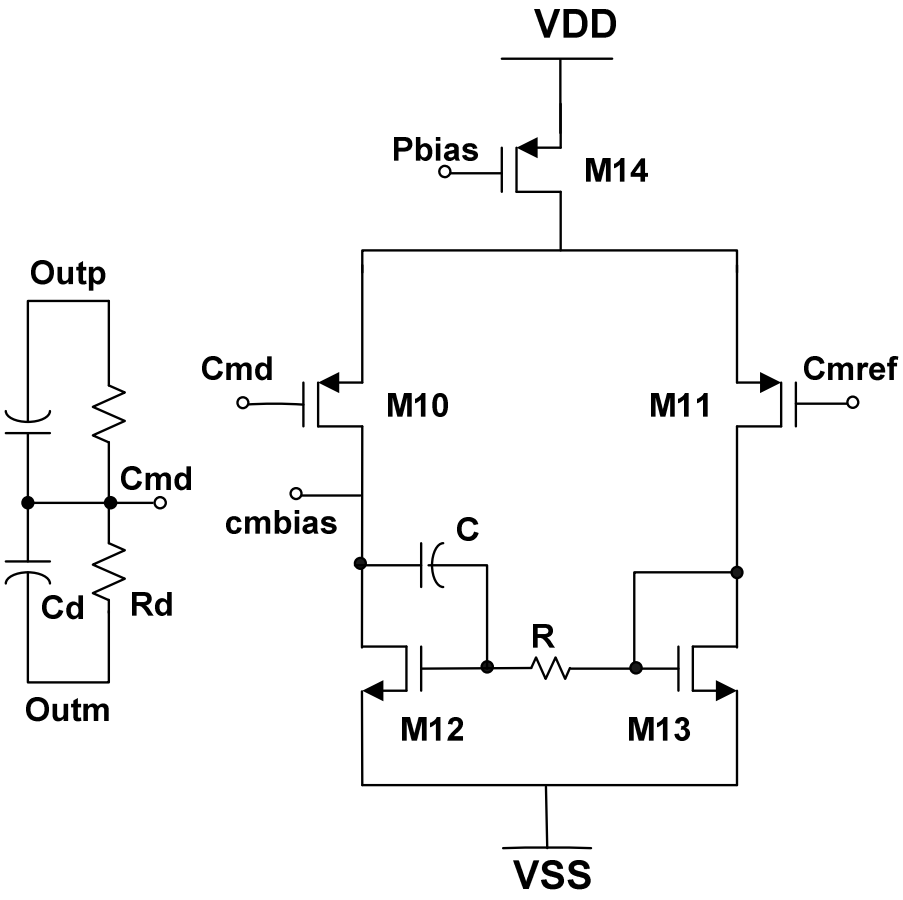


Fig. 4.8 Common mode feedback amplifier for integrator 1 and integrator 2

The common mode amplifier (M10-M14 in Fig. 4.8) used in this setup exhibits high gain at lower frequencies and a mid frequency pole zero pair. High low frequency gain of the CMFB amplifier results in an accurate control of DC common mode values. This amplifier is similar to the one used for the filters described in chapter II of this dissertation. Detailed characteristics of this amplifier are discussed in chapter II.

4.4.2 Simulation Results: Integrator 1

Fig. 4.9 shows the magnitude and phase response for amplifier 1.The simulation is carried by opening the feedback around amplifier 1 while loading it with the integrating capacitor. Extension of Unity Gain Bandwidth is evident due to the in-band real zero (around 100MHz) realized through nulling resistor Rc and Cc (in Fig. 4.7). The unity gain bandwidth and the phase margin are 1.4GHz and 45degree respectively. The real zero is placed in band in order to recover the phase loss below 250MHz (half-sampling rate).

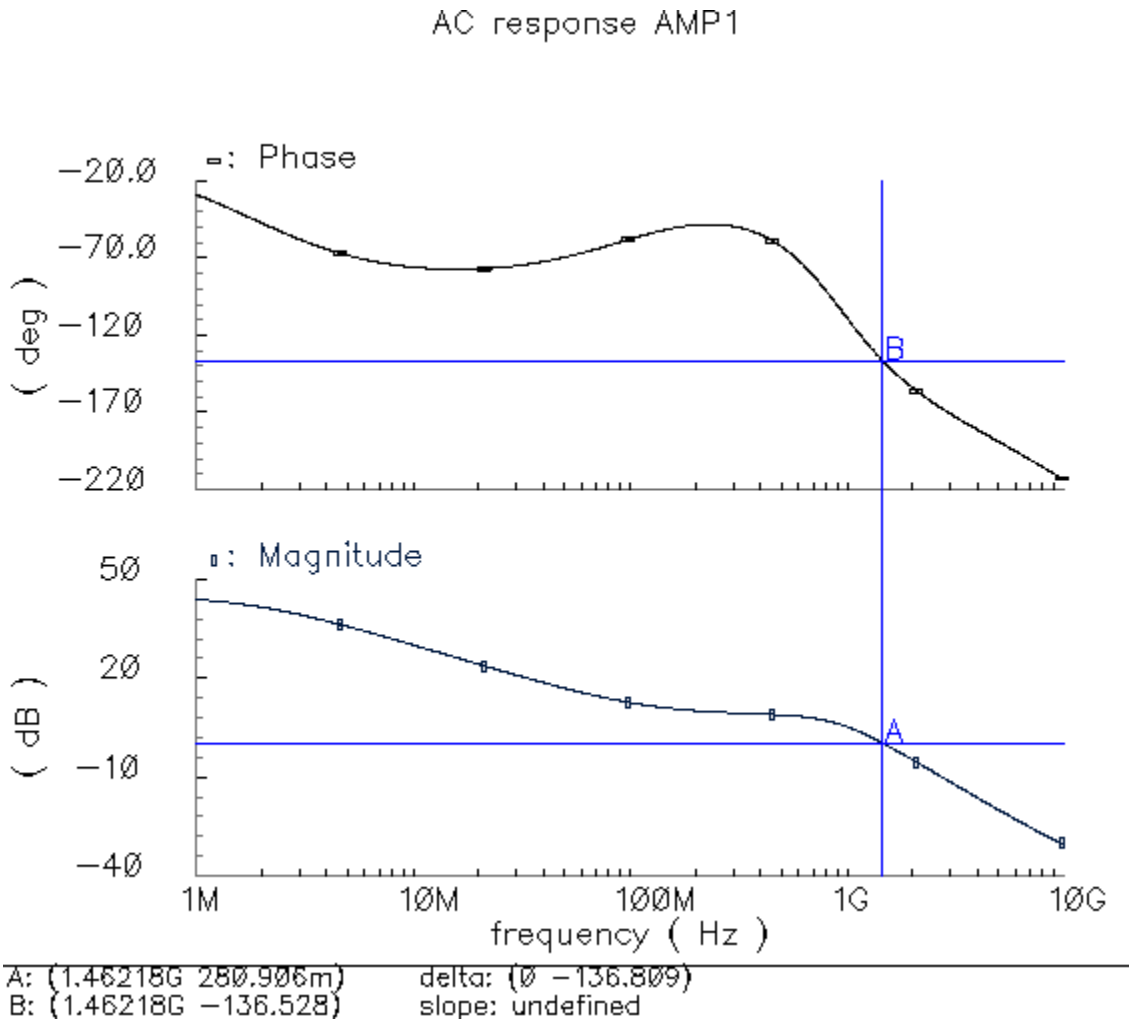


Fig. 4.9 AC response for amplifier 1

In order to ascertain the stability of the common mode feedback loop, this loop is opened at the output of the common mode detector. The small signal response (magnitude and phase) for the common mode feedback loop is plotted in Fig. 4.10. The unity gain bandwidth and the phase margin are obtained to be 67MHz and 72 degree respectively.

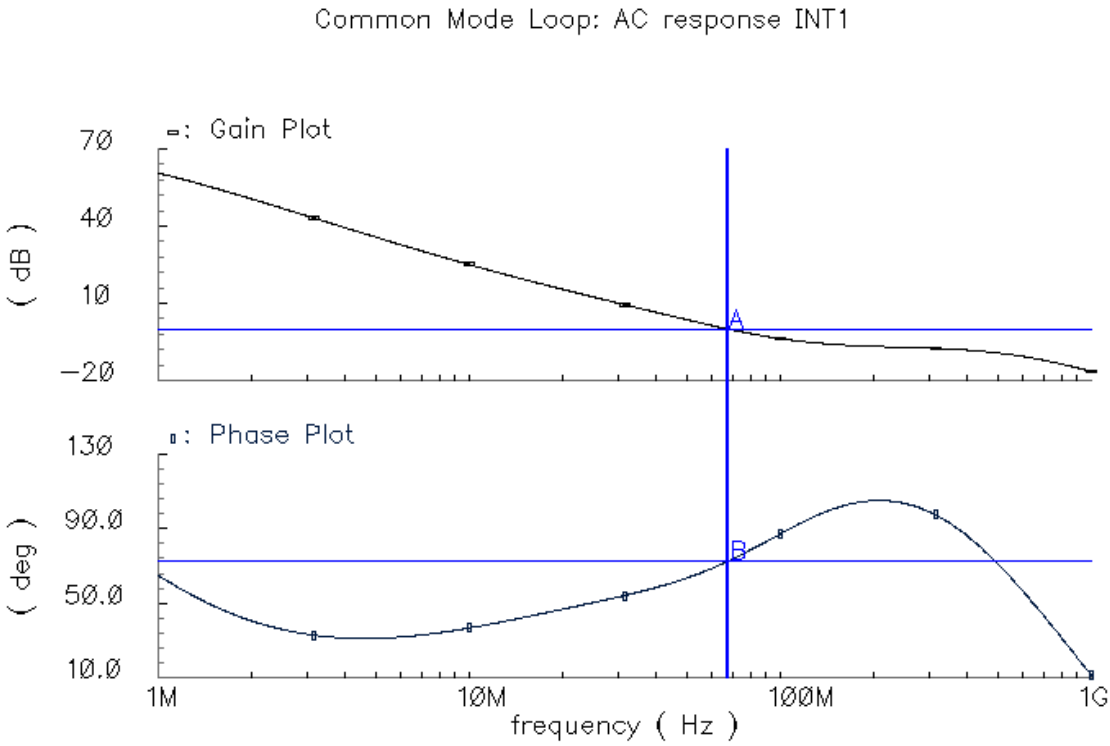


Fig. 4.10 Magnitude and phase response of the common mode feedback loop for amplifier 1

The open-loop response of the common mode feedback loop, though a necessary test to ascertain stability, may not reveal any transient issues associated with the loop (bias weakness across swing, slew and transient induced instability). Instead, fast and large steps of common mode currents are injected at the output port and the settling behavior of the common mode loop is observed. Fig. 4.11 shows the corresponding setup. Pulsed current sources I_cm are connected to each of the outputs of the amplifier. These sources inject stepped in-phase current and thus perturb the steady state common mode voltage using a fast moving transient. Outputs of the amplifier can then be observed to ascertain the settling behavior of the common mode loop.

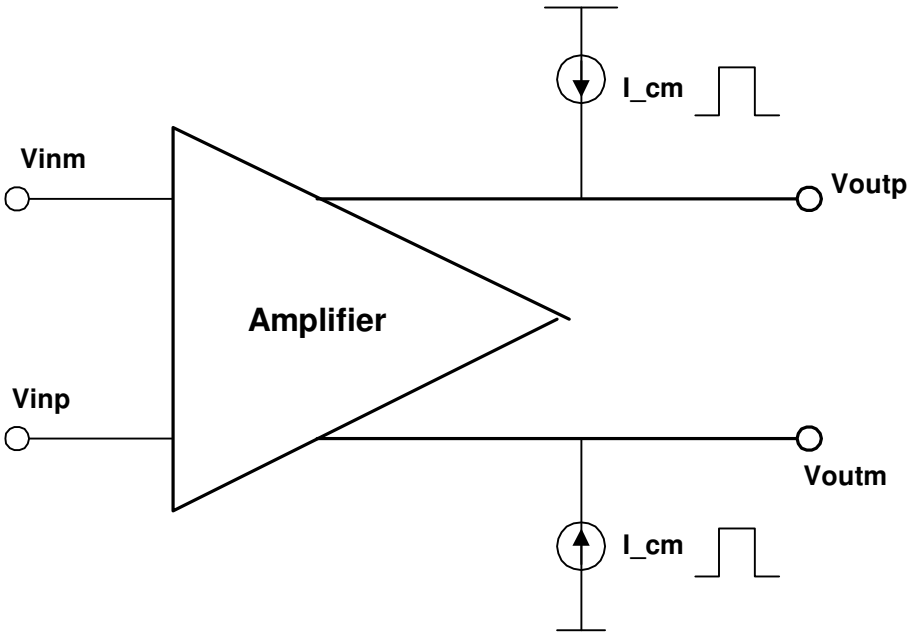


Fig. 4.11 Simulation setup for characterizing step response of common mode feedback loop

Fig. 4.12 shows the simulated settling response for the common mode feedback loop. The applied current (I_cm) is stepped between 0-60uA. It is shown through the output settling that the common mode of the amplifier is well behaved and settles within 100ns of the current transient.

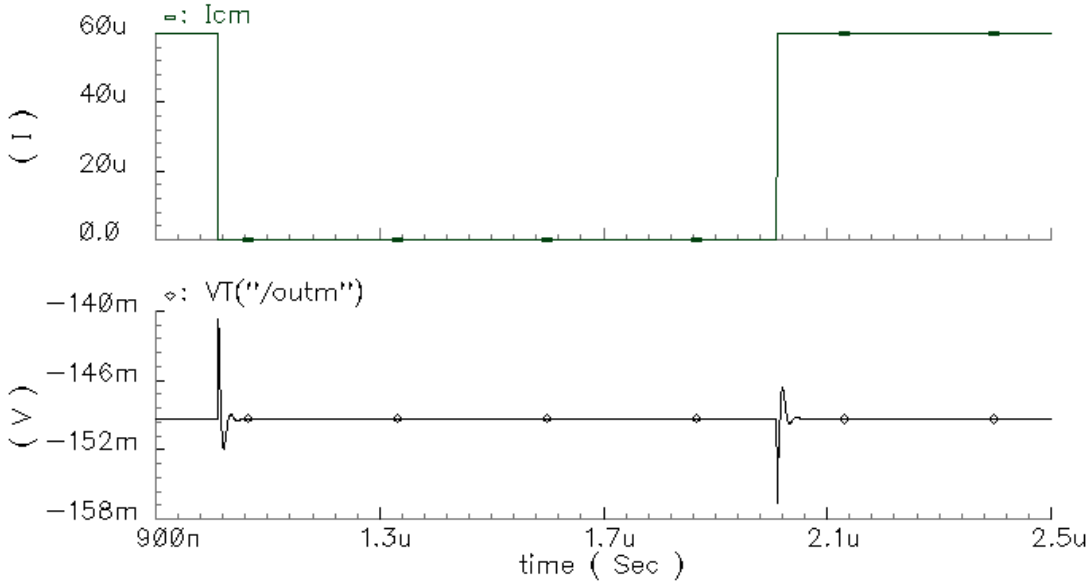


Fig. 4.12 Common mode settling behavior for amplifier 1

Fig. 4.13 shows the output of integrator 1 when a two tone input (17.5MHz and 18.5MHz) is applied. As discussed earlier, integrator 1 has to support a high output swing of around 400mV p-p differential. Fig. 4.14 shows the corresponding spectrum output. The resultant IM3 is shown to be around 65dB. Note that in real systems performance may be better than the simulated linearity. In real system most of the input and output swing for integrator 1 is high frequency transient (unfiltered quantization noise). Whereas, in the simulated case, pessimistically, signal swing is emulated by applying power distributed in two in-band signal tones.

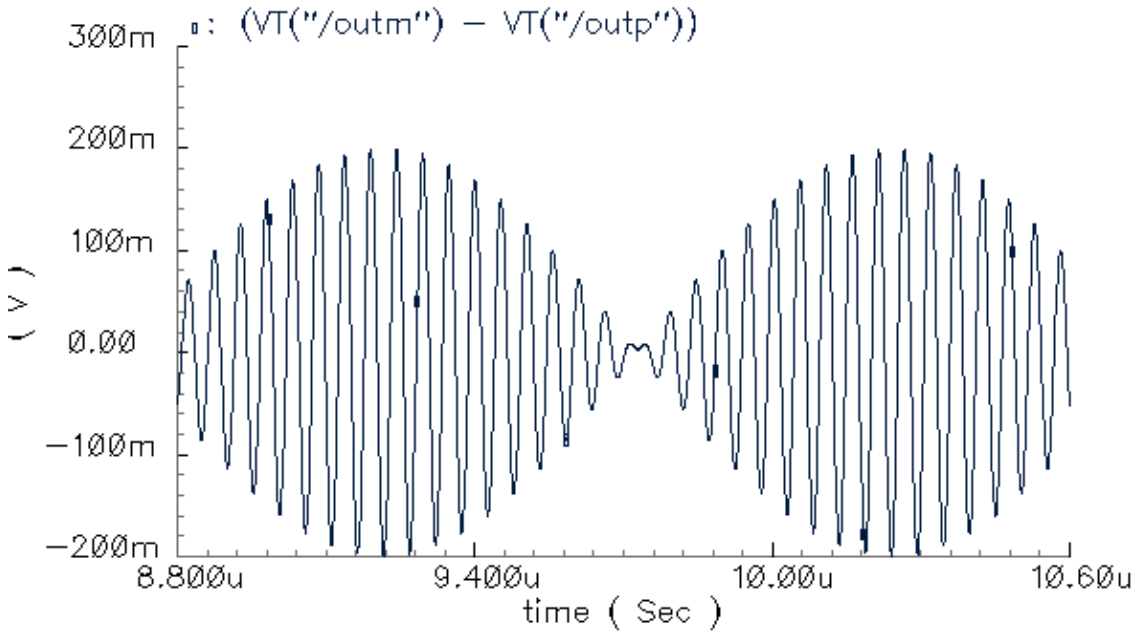


Fig. 4.13 Output transient waveform for integrator 1: two tone input

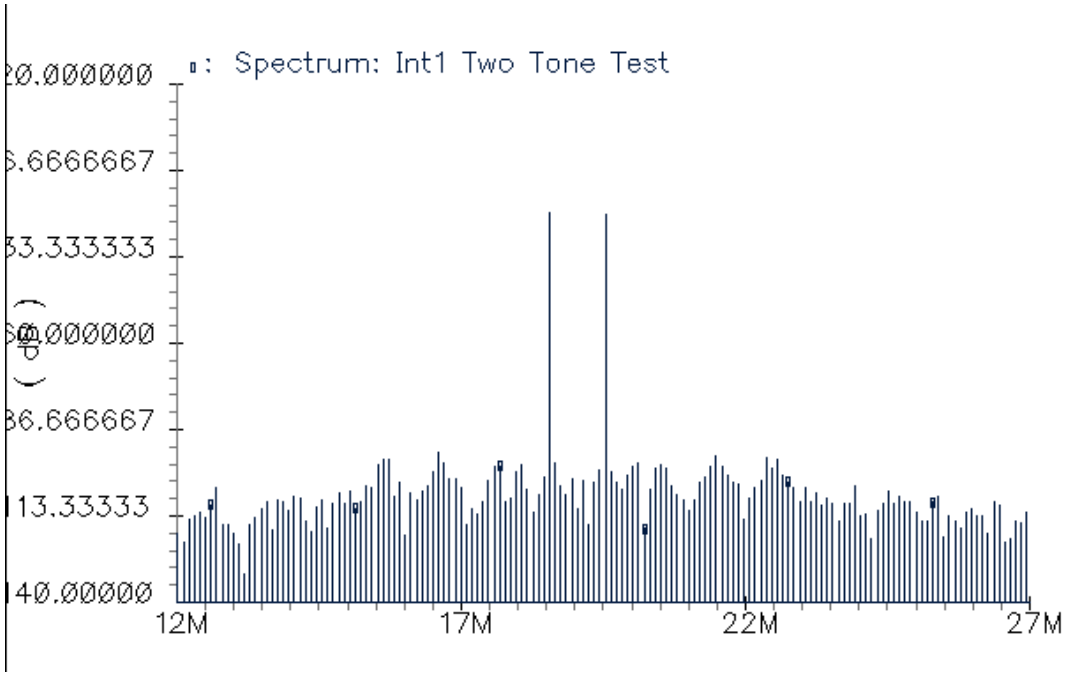


Fig. 4.14 Output spectrum: two tone input for integrator 1

4.4.3 Integrator 3: Amplifier Architecture

Apart from inputs from the biquadratic block (through R3, C_H and C_B in Fig. 4.6), integrator 3 also processes a forward path from the time-quantizer termed Kfb. Kfb path is provided in order to stabilize the loop in presence of excess loop delay and unavoidable excess phase introduced through the biquad and TDC.

In order to compensate for the excess delay due to filter and TDC, Kfb path needs to provide low phase direct feedback around the quantizing element [44]. Through system simulations, maximum loop delay for the ADC is specified to be 500ps; of which TDC and PWM could account for 400ps. This implies that the maximum allowable pulse delay from the Kfb path is 100ps specified at 250MHz. Thus, group delay compensation path should have fast response with excess phase less than 10 degrees at 250MHz. For practical implementation of the fast feedback around the quantizer, current proportional to differentiated DAC code is injected at the virtual ground of the third integrator through a switchable capacitor bank Cfb. Fig. 4.15 shows the Kfb path along with integrator 3. To ensure low excess phase for Kfb path, through the third integrator, following techniques are employed:

a) Use of coupling capacitors Cfb ensures that the injected signal from quantizer avoids integration inherent due to C3.

b) Architecture for third amplifier is carefully chosen such that it adds minimum possible excess phase and provides a fast response.

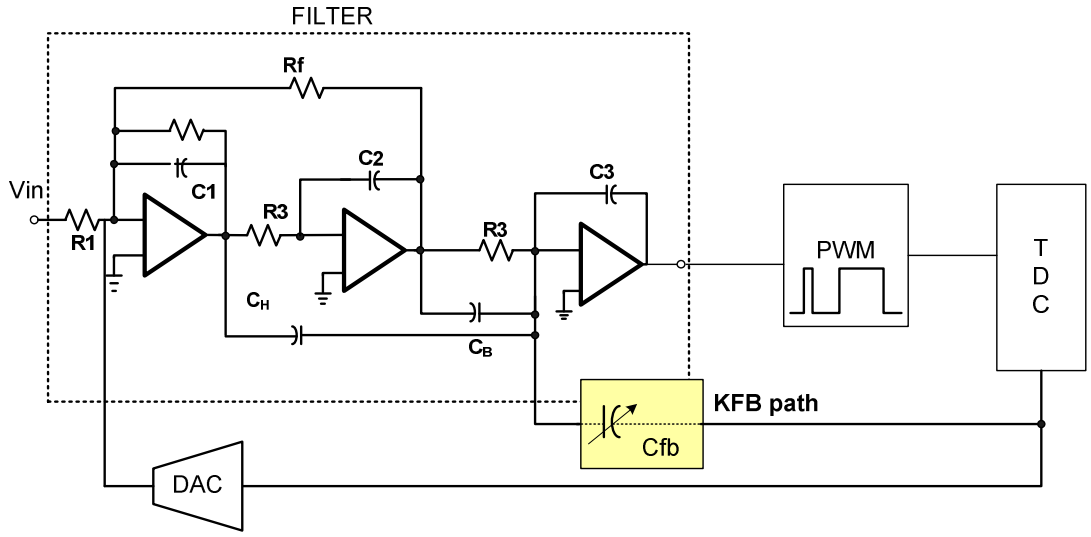


Fig. 4.15 Excess loop delay compensation: Kfb path

As discussed above, the third amplifier needs to have a wideband response for effective compensation of excess phase (through Kfb path). One of the fastest possible amplifier architecture is a pseudo-differential inverter-based structure as shown in Fig. 4.16. This structure does not have any internal nodes apart from the input and the output ports.

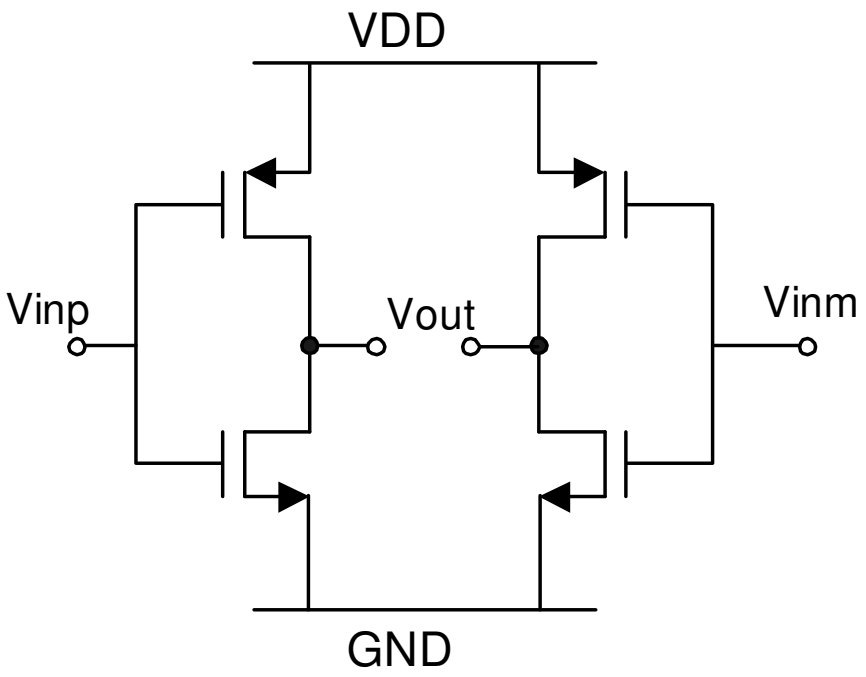


Fig. 4.16 Amplifier architecture based on an inverter

To justify the choice of such architecture following observations are made:

a) Such inverter based architecture exhibits maximum possible gain-bandwidth for given capacitive load. Absence of any signal nodes besides input and output ports makes this simplified structure an ideal candidate for a wideband amplifier.

b) It was discussed in previous sections of this chapter that a gain of 8 is incorporated in the biquad that precedes the third integrator. Thus, the DC gain requirement for the third integrator and hence the amplifier is relatively modest. Thus, single stage amplification is sufficient for the purpose.

c) Because of its pseudo-differential nature, this amplifier has poor common mode and supply noise rejection. However such disturbances associated with this architecture are attenuated through the biquad gain when referred to the input of the filter. A gain of 8 that was incorporated in the preceding biquad relaxes the supply noise specifications for this amplifier and allows for a simpler pseudo-differential architecture. For example, for a supply rejection ratio of merely -6dB (0.5) for this amplifier; the supply rejection referred to the input of filter would be $\frac{0.5}{64} \sim \frac{1}{128} \sim$ -42dB.

4.4.4 Common-Mode Feedback Architecture for Amplifier 3

Due to lack of controllable current source in the inverter based amplifier, atypical architectures for common-mode-control need to be used. The scheme employed here controls the input common mode by injecting small controlled current at the amplifier input [45]. The basic architecture is shown in Fig. 4.17. Output common mode of the amplifier (Vcm) is detected through RC network. Detected common mode, Vcm, is compared to the suitable reference (Cmref) to generate an error voltage. Current sources labeled Icm are controlled through the common mode error signal (Verr) fed by error amplifier EA. Common mode currents Icm injected to the virtual-grounds of the amplifier control input common mode of the amplifier through R3. Following equations describe the common mode control:

$$Vcm = Vincm*TF_3 \quad (4.8a)$$

$$Vincm = Icm*R3 \quad (4.8b)$$

TF_3 represents the transfer function of the third amplifier. Icm is related to Vcm through transconductance ratio.

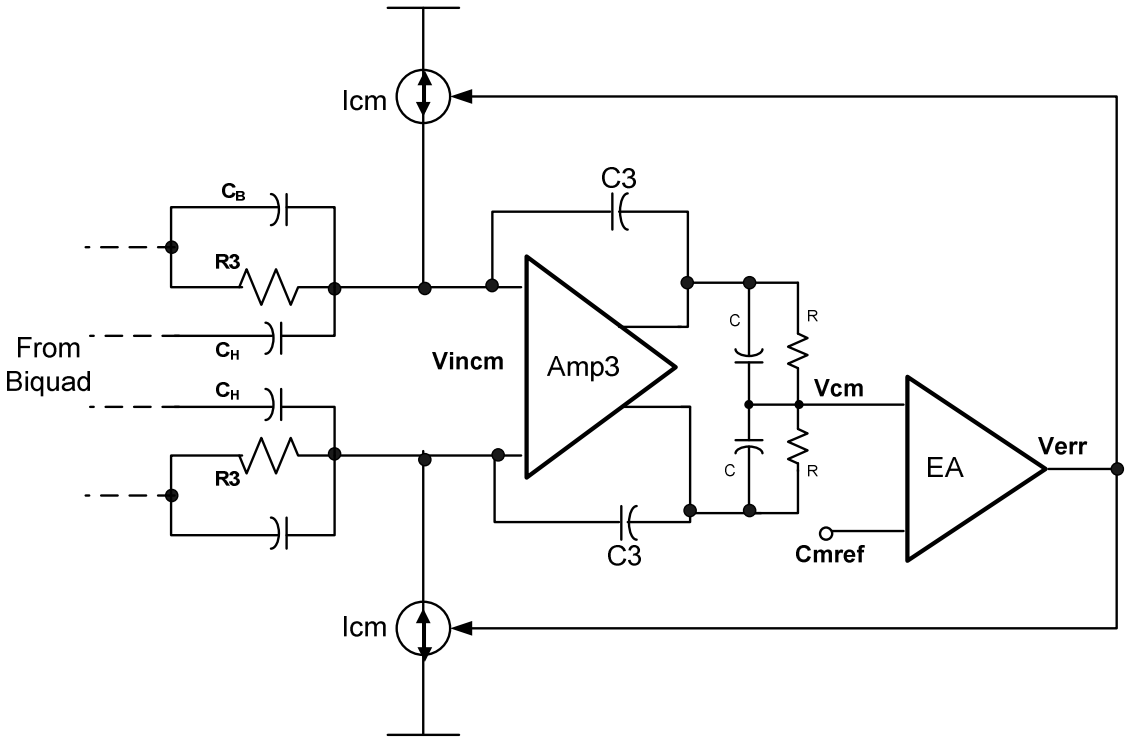


Fig. 4.17 Common mode feedback architecture for integrator 3

Fig. 4.18 shows the detailed schematic for the common mode control of integrator 3. M1-M2 constitute the core inverter based amplifier. M3-M4 form the current source Icm for common mode control. Since output common mode (and hence cmref) for integrator 3 is set at half supply, Error Amplifier (EA) is also based on a pseudo differential structure. Lack of tail current source enables EA's drivers to be biased at mid rail levels.

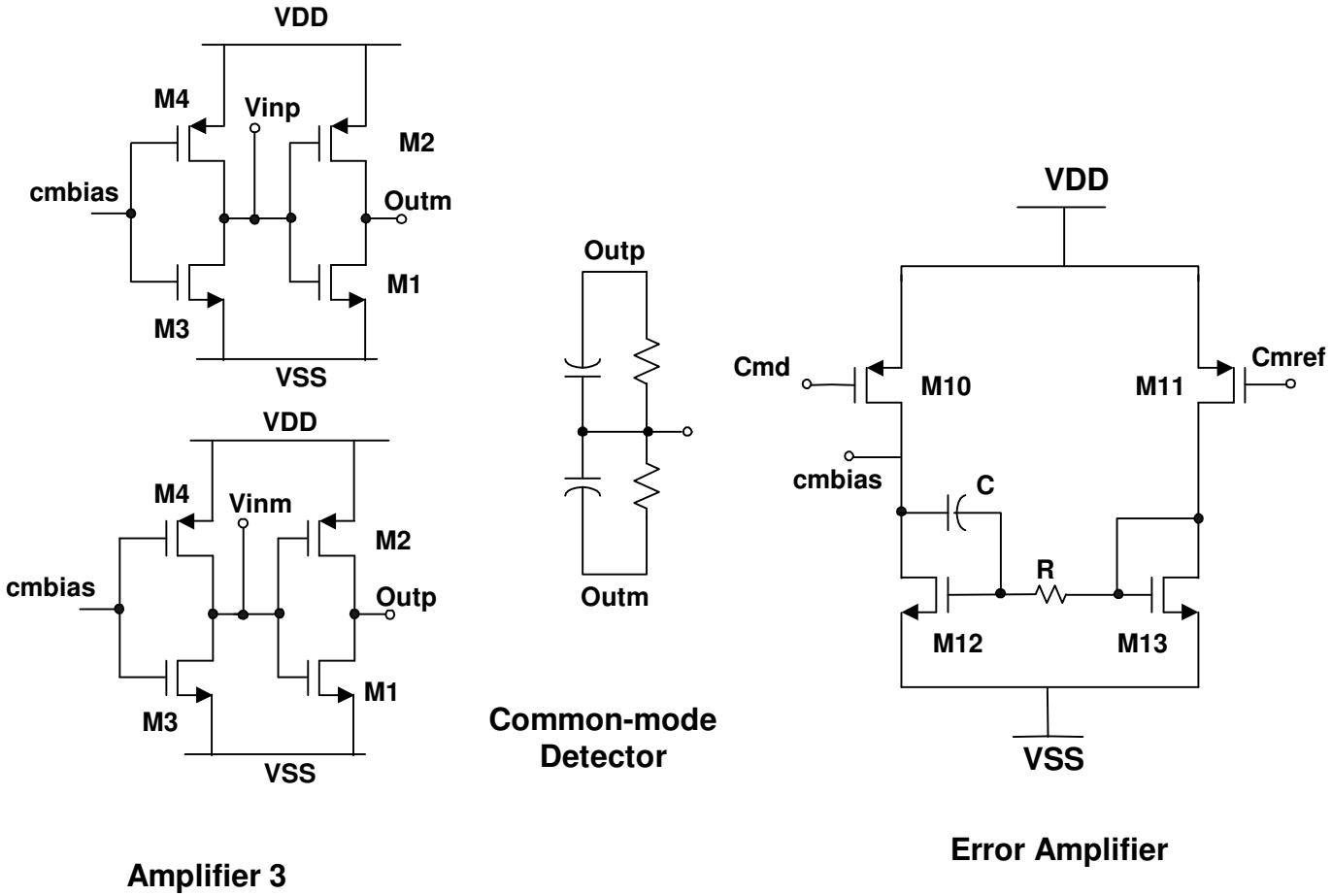


Fig. 4.18 Schematic for amplifier 3 and its common mode feedback

Note that even though transistors M4-M5 realize a small current source - hence have a small transconductance - they are sized large (large L, small W/L) in order to meet the flicker noise requirements. Table 4.4 outlines device sizes and component values for the third amplifier.

Table 4.4 Device dimension for amplifier 3

M2	**M1**	**M4**	**M3**	**M10-11**	**M112-13**	**C/R**
8(11/0.15)	8(4/0.15)	2(2.8/6)	2(1.4/6)	3(8/0.3)	3(4/0.3)	800f/60K

4.4.5 Simulation Results for Integrator 3

Since amplifier 3 does not have any additional nodes (apart from input and output); its gain-bandwidth can be designed to be as high as a few GHz. In this context it is more useful to plot the third integrator's (closed-loop) magnitude and phase response. Fig. 4.19 outlines magnitude and phase response for third integrator's differential (closed-loop) path. As expected, integrator 3 exhibits negligible excess phase around 250MHz (half of the sampling-rate).

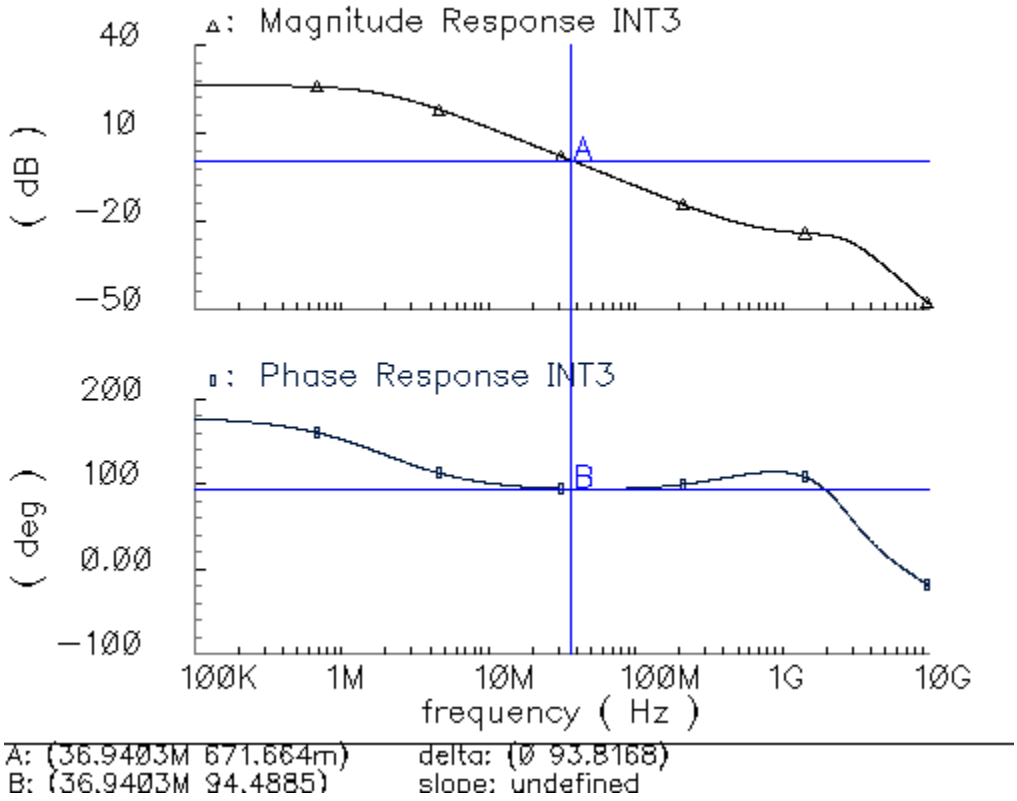


Fig. 4.19 Magnitude and phase response of integrator 3

Fig. 4.20 shows the magnitude and phase response of the common mode feedback loop associated with the third integrator. Unity gain bandwidth and phase margin for the common mode path are 23 MHz and 78 degrees respectively. Fig. 4.21 shows common mode settling in response to current excitations applied at the output. Common mode step current of 200uA, which is 10% of the amplifier quiescent current, is applied. It can be seen that output settles in response to the current step within 180ns.

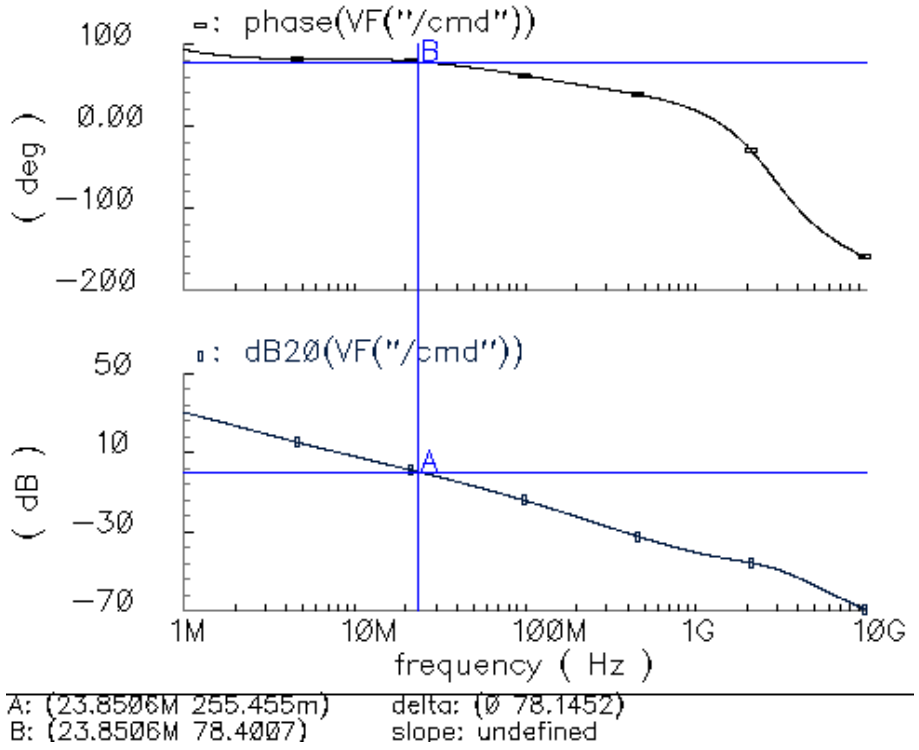


Fig. 4.20 Open loop response of common mode feedback for amplifier 3

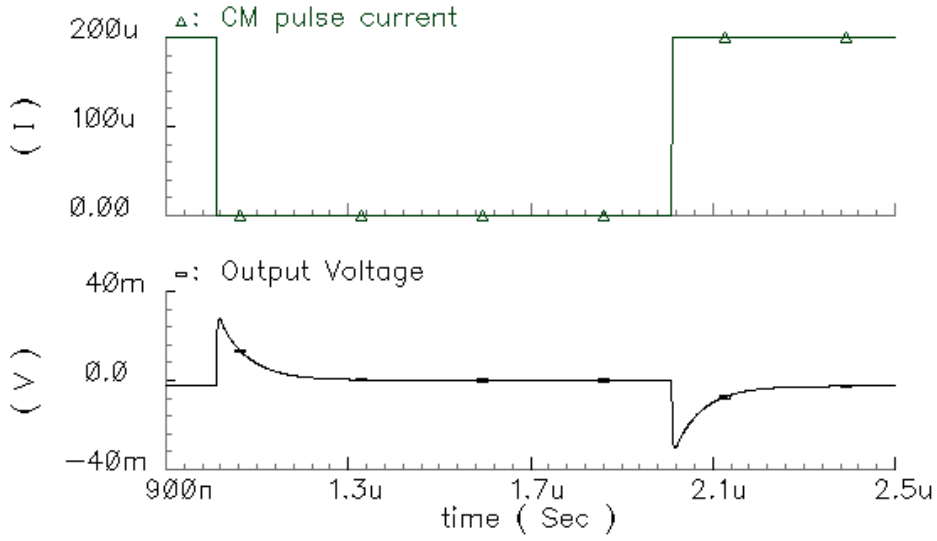


Fig. 4.21 Common mode step response for amplifier 3

Fig. 4.22 shows the output of integrator 3 when a two tone sinusoid input is applied to it. Frequencies of the two sinusoid are centered around 18MHz. Amplitude of the tones is adjusted so as to have the rated 770mV p-p differential swing at the output of the integrator. The corresponding spectrum shown in Fig. 4.23 that indicates IM3 of 65dB.

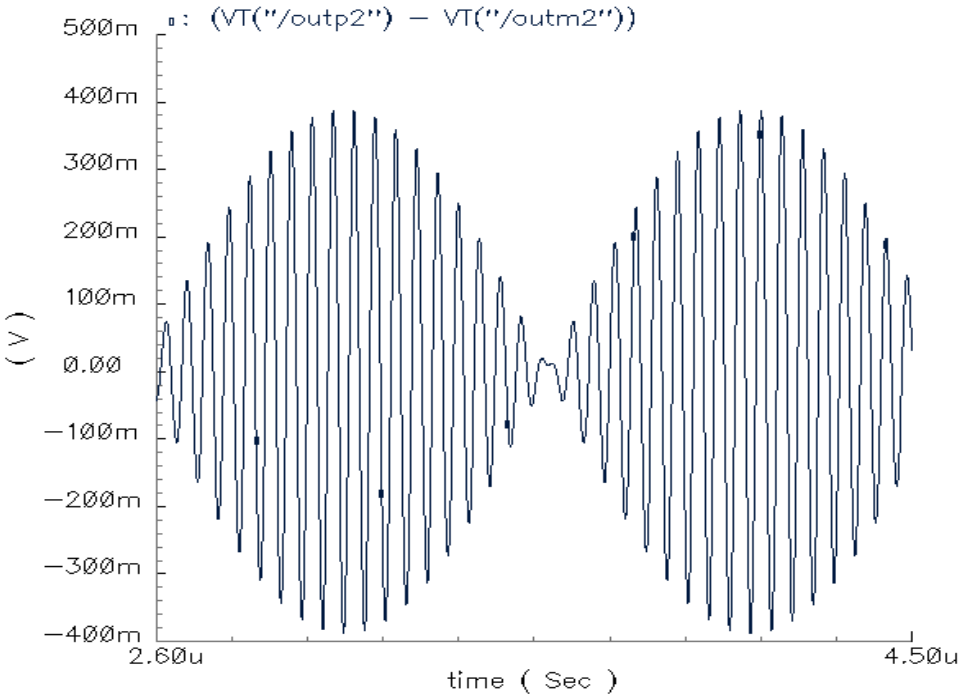


Fig. 4.22 Integrator 3 output: two tone response

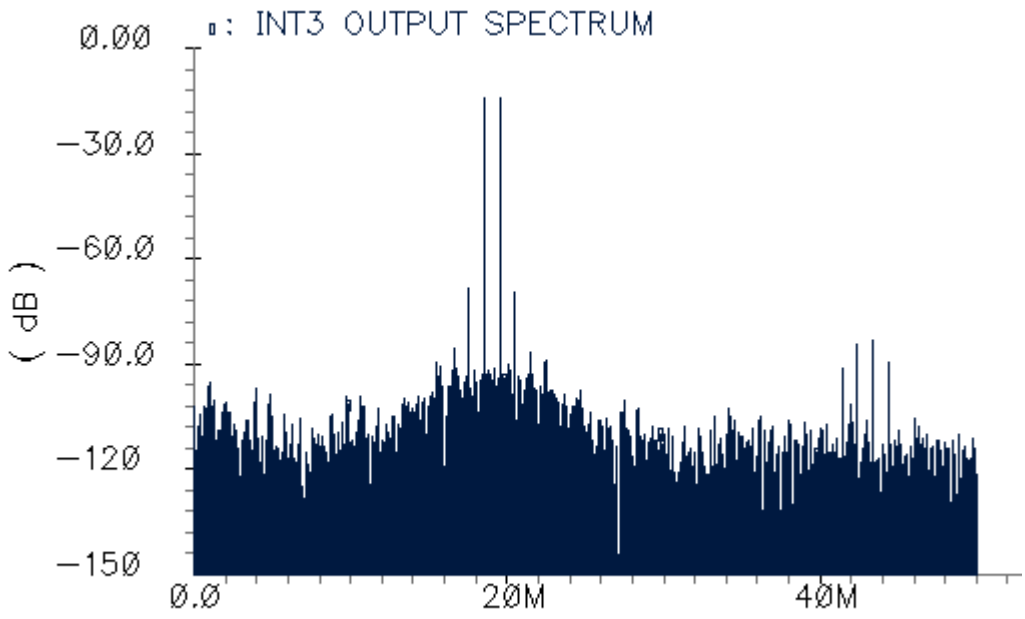


Fig. 4.23 Spectrum for integrator 3: two tone input

4.5 Filter Verification: Simulation and Experimental Results

4.5.1 Simulation Results

Top level simulations of the filter include verification of multiple paths:

a) Main filtering or forward path

b) Kfb loop compensation path

c) DAC feedback path

In order to ascertain transfer characteristics of main and feed-forward kfb paths, filter time constants are tuned to their nominal value and kfb coefficient is centered to compensate for the nominal delay due to TDC (500ps). AC signal is applied to each of

the paths and the resulted gain and phase plots are verified against the ideal response. Fig. 4.24 compares the gain response of the two paths.

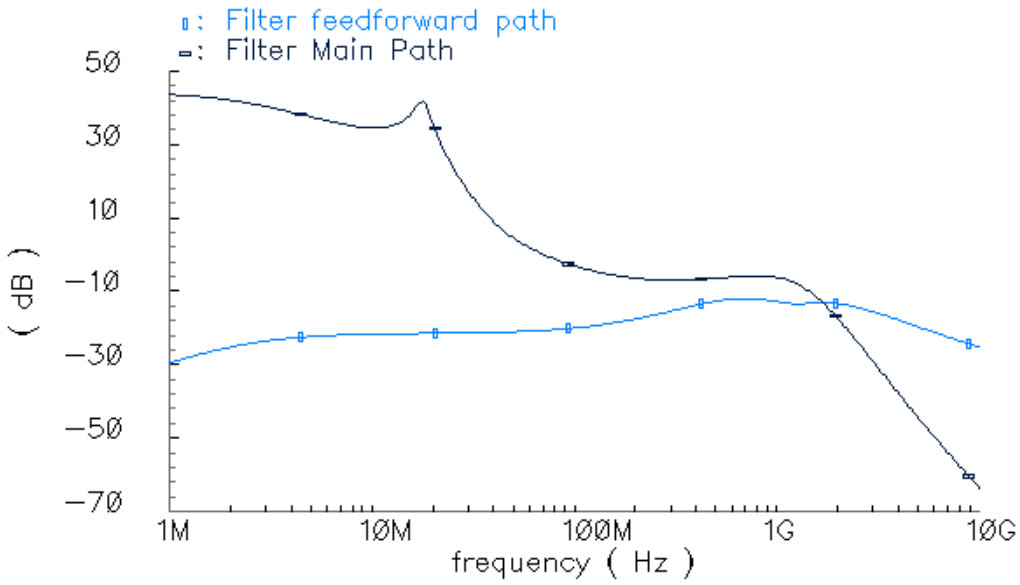


Fig. 4.24 Gain response: main filtering path and feed-forward Kfb path

It can be observed that for higher frequencies (> GHz) Kfb path dominates between the two: it provides the necessary loop gain and maintains the phase at such frequencies. For varying loop delays, Kfb coefficient can be tuned and its gain plot adjusted in reference to the main filtering response.

In order to test for the transient performance of the filter, the loop around the third order filter is closed using a unity feedback (which emulates closing of loop through the delta sigma structure). This setup ensures stable transient points and prevents

saturation for integrators as the input transients are applied. Fig. 4.25 shows the sinusoid (6.8MHz) output with the rated swing of 770mV p-p differential.

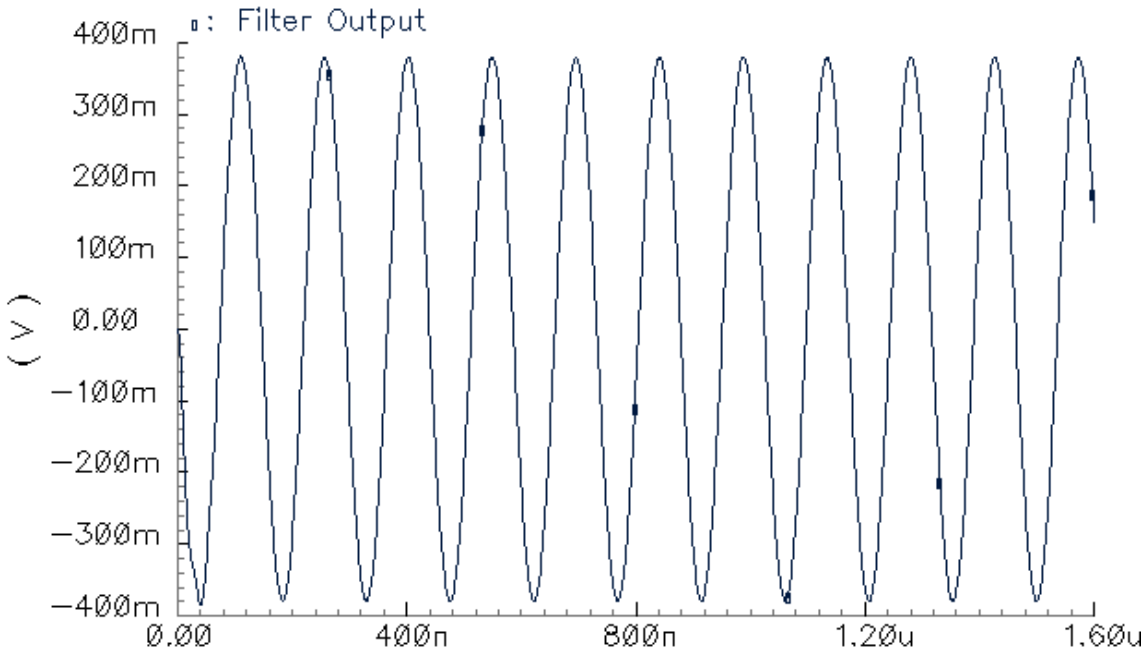


Fig. 4.25 Output of the filter for 6.5MHz sine wave input

Fig. 4.26 and 4.27 show the output spectrum of the filter for single tone and two tone inputs respectively. For single tone 6.5MHz sine wave, third order harmonic distortion of 72dB is observed.

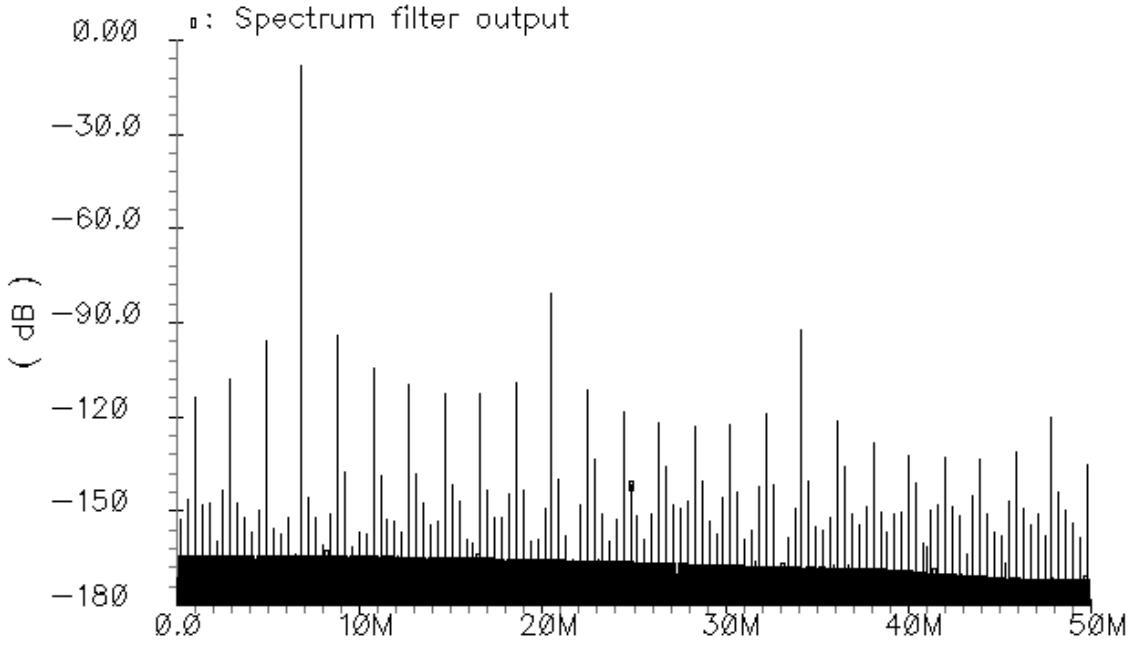


Fig. 4.26 Spectrum output for a single tone input

For the two tones spectrum shown in Fig. 4.27, IM3 (third order intermodulation ratio) is observed to be around 67dB. For the two tone test, amplitude at the output of the filter is maintained close to the rated value of 770mV p-p differential at the output of the filter.

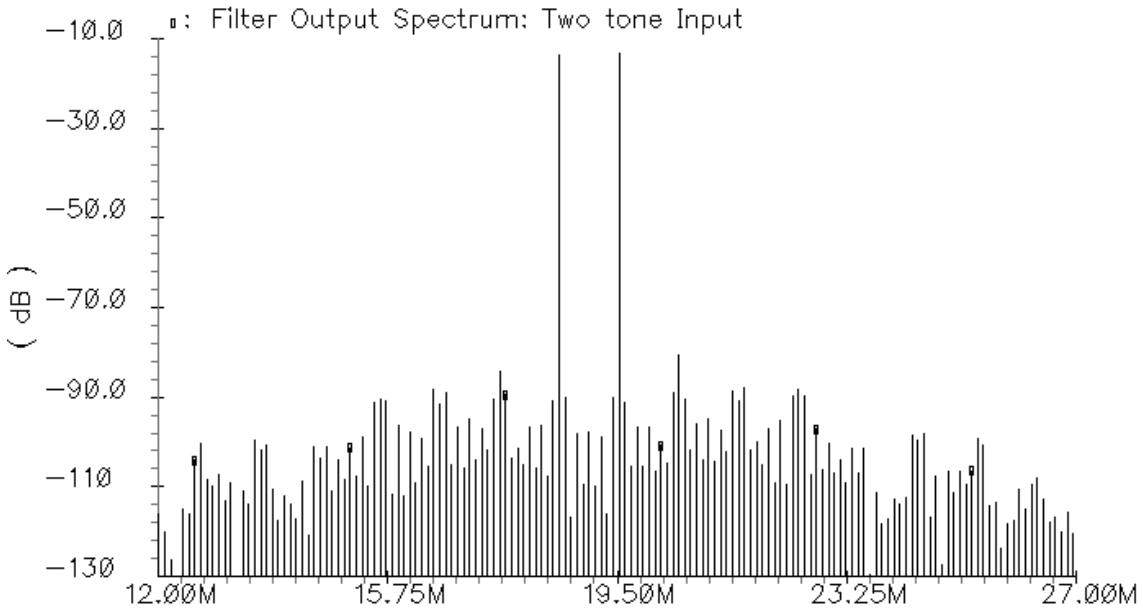


Fig. 4.27 Spectrum output for two tone inputs at 17.5 and 18.5MHz

Finally, DAC path connected to the filter is verified by applying pulses to the input of DAC transconductor that feeds to the virtual ground of integrator 1. This steps the current injected at the virtual ground of integrator 1 by 160uA single ended. The resultant settling behavior is shown in Fig. 4.28. It can be seen that the filter settles well within 260ns and the current step results in 770mV p-p differential voltage swing (which is also the maximum rated voltage swing at the output of the filter).

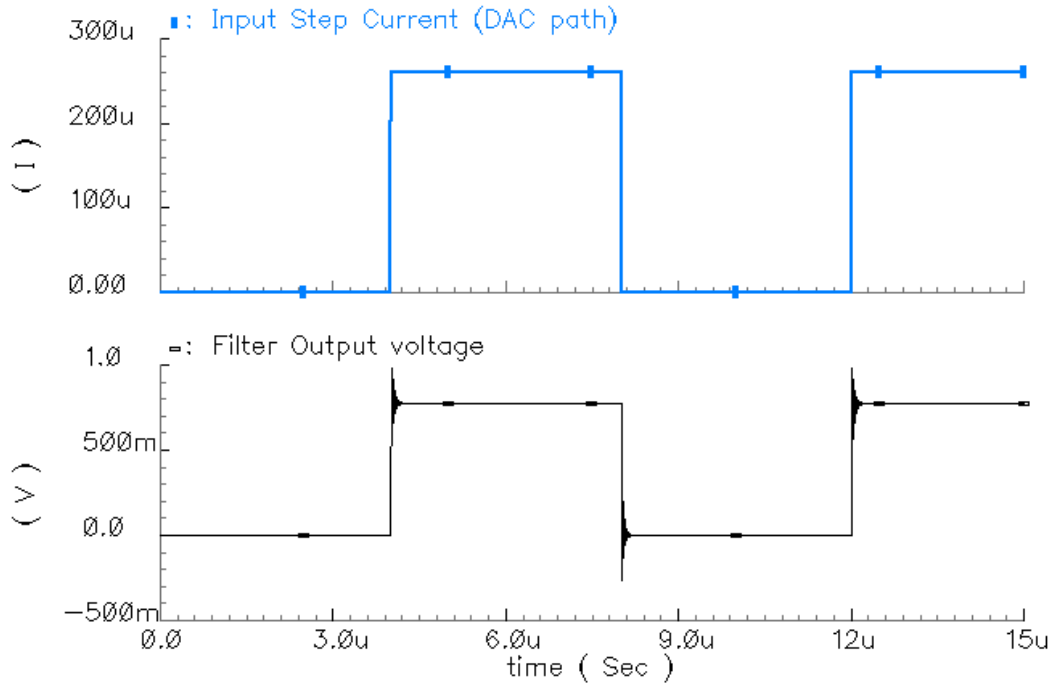


Fig. 4.28 Filter's response to the stepped current from the DAC

4.5.2 Experimental Results

The filter prototype was fabricated as a part of WLAN ADC using TI 65nm CMOS technology. The chip micrograph is shown in Fig. 4.29. The ADC occupies an area of .15mm^2, of which the filter occupies almost half of it.

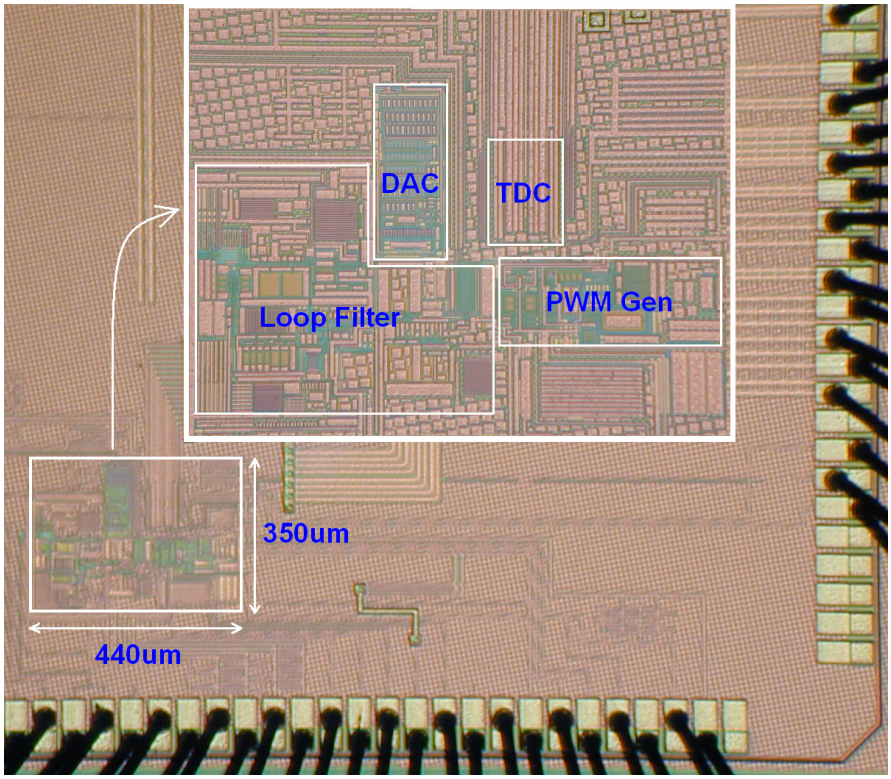


Fig. 4.29 Chip micrograph

Since the fabricated filter is part of a continuous time delta sigma ADC, its coefficients need to be tuned in order to take into account process shifts and excess loop delay. To ascertain process variation (on chip RC constants), a test structure consisting of a resistor and capacitor (similar to one that determine integrators' time constant) was fabricated within the IC. Process variations in RC time constant are estimated by probing the pads through a multimeter and network analyzer. The fabricated RC time constant was found be only 10% slower than the expected nominal value. Each of the integrators RC components are tuned accordingly (by switching correct resistor and capacitor value from a bank of components). A pattern generator is used to program the digital control

bits. Fig. 4.30 shows the test setup and the measurement board. A signal source (Agilent E4432B) is followed by a high-Q, passive, LC bandpass filter (that filters signal harmonics). ADC output is captured through an on chip LVDS interface and logic analyzer.

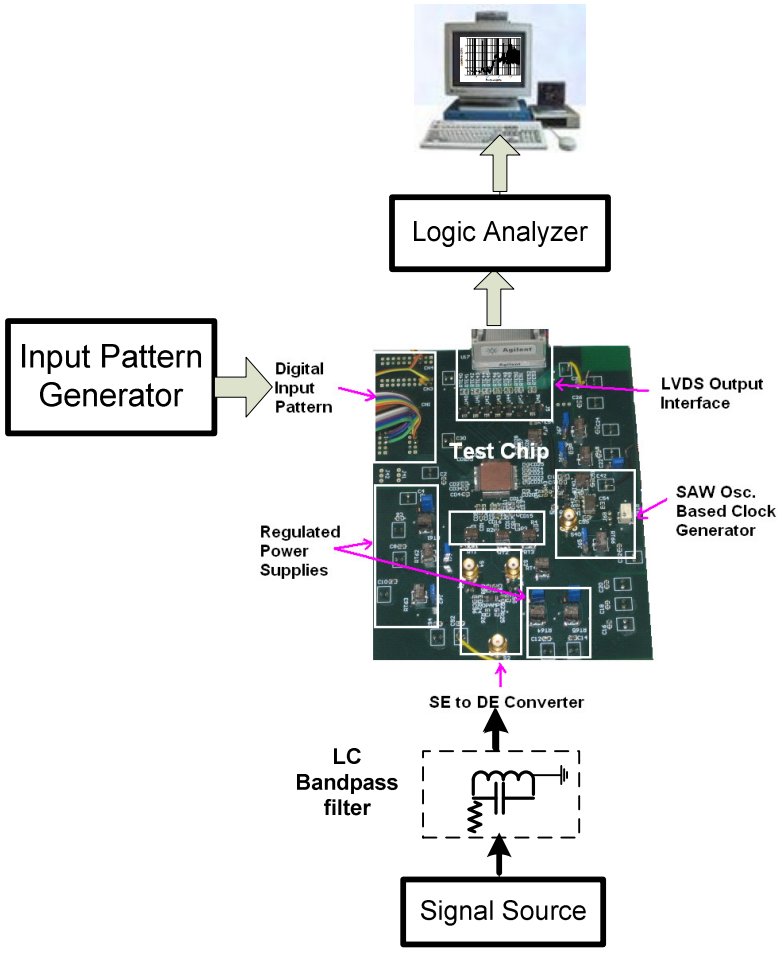


Fig. 4.30 Test setup for characterization of the ADC

Digital output, thus captured is processed through MATLAB and resulting spectrum is plotted in Fig 4.31. The noise shaping apparent in the curve verifies the functionality and the transfer characteristics of the fabricated filter.

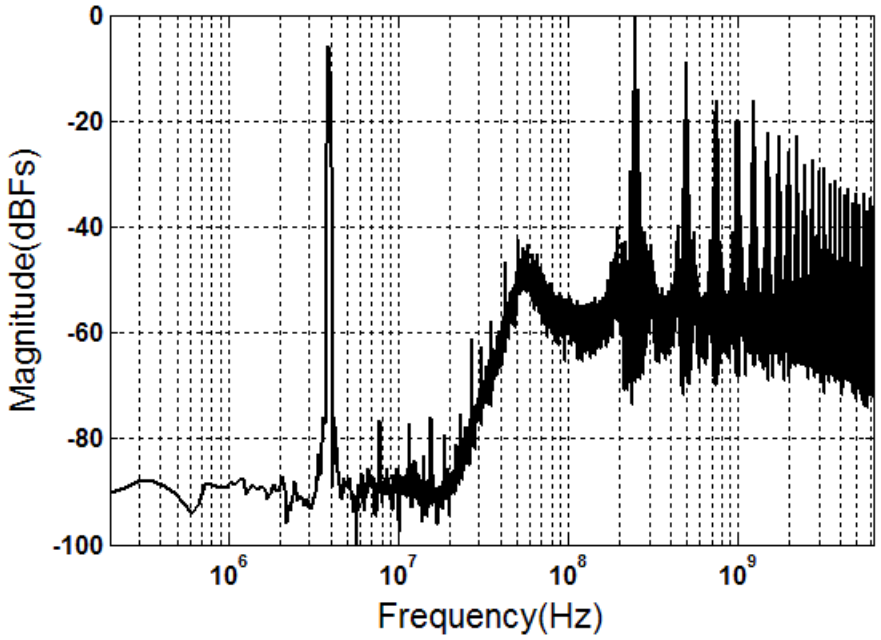


Fig. 4.31 Output spectrum of the ADC

Peak SNR and signal to noise and distortion ratio (SNDR) for the ADC are measured to be 62dB and 60dB respectively and are observed at input level of -5dBFs. The peak total harmonic distortion (THD) for the ADC is about 67dB and is observed at -6dBFs input level. These measured results closely match the design and simulation. Power consumption for the ADC is 10.5mW; of which the filter consumes 5mW of power. Power consumption of the entire system is competitive against similar ADCs reported so far [46-0]; and is projected to outperform with further scaling in CMOS

technology. Since, block power split-up is usually not reported; it is difficult to compare stand-alone filter's power to ones reported for similar ADCs.

4.6 Conclusions

This chapter presented the design and implementation of a third order active RC filter for a 20MHz continuous time, digital friendly, ADC architecture. Filter architecture was carefully chosen for its suitability to scaled digital CMOS technologies. In order to minimize excess phase for a stable operation of the delta sigma loop, use of an ordinary inverter as amplification element was explored. Also presented were some key ideas for control of common mode for such amplification schemes.

The third order filter presented here is one of the few analog blocks remaining in the digital-centric ADC architecture. While the power of the digital subsection of this ADC is projected to scale down with finer CMOS technology, the analog filter may prove to be a bottleneck for reducing overall system power. Future research directions may include use of low performance amplifiers and either compensating their non idealities or devising methods to work around them. This design utilizes digital inverter based amplifier for the last stage of the filter. Use of this amplifier in earlier stages was prevented by performance limitations this structure imposes. If, however, techniques are developed that enable the use of such an amplifier for the entire filter, the scalability of the filter architecture with technology can be ensured.

CHAPTER V

CONCLUSIONS

5.1 Summary of Research

This dissertation presents novel architectural and circuit solutions for design of low power filtering blocks. Initial chapters of this dissertation are dedicated to wideband filtering techniques (a few hundred MHz to GHz range) for disk drive and data communication applications. An efficient architecture for implementation of wideband equalizing filters has been proposed. Gm-C implementation based on this architecture is shown to be at far more efficient than any other equivalent design. This particular filter has been designed for bandwidth of 330MHz with 24dB equalization gain. An LC implementation of this architecture is also compared to the Gm-C approach. It is concluded that for typical applications (moderate bandwidth and SNR) LC approach, though consumes less power, occupies much larger area. Subsequently, this dissertation develops techniques based on complementary devices that can improve power efficiency of Gm-C based structure by almost a factor of seven. The realized filter based on this approach has bandwidth of 1.3GHz, SNDR of 54dB and consumes power of merely 22mW. Finally, filter design techniques suitable for continuous time delta sigma ADC realized in deep submicron digital CMOS technology are discussed. The third order active RC filter implemented for such ADC consumes 5mW of power for a 20MHz application with SNDR of nearly 68dB.

5.2 Area for Future Work

For most systems, integrating the analog blocks along with the digital core in deep submicron technologies yields a lower system cost; albeit at the expense of increased complexity. Such integration usually negatively affects the power efficiency of core analog blocks, mostly due to reduced signal swing and dynamic range.

This dissertation presents filter solutions that are aimed at improving the overall power efficiency while remaining suitable for integration in fine line CMOS. Key ideas regarding inverter-based current mirroring block and amplifiers, which scale well with digital CMOS technologies, are applied with regards to specific filters. There are many challenges that prevent the widespread use of such class of 'inverter-based' analog circuits. A few of these problems are addressed in this work. For example, signal processing in current-domain was employed to overcome supply sensitivity of inverter based structure for a particular class of low Q filters. Generic use of power efficient and scalable analog blocks along with or without calibration can form basis of future research.

Wideband filters (equalizing and current-mode) included in this dissertation are presented as a proof-of-concept for novel architectural or circuit techniques that significantly improve power efficiency. Additional features such as automatic tuning and wide range programmability are not included in the prototypes. Future scope of work may also include investigations regarding optimum programmability and tuning mechanism.

REFERENCES

1. G. MacGillivray, "Hard-disk drives vs. flash," EE Times.com, Jan 2006. [Online]. Available: http://www.eetimes.com/showArticle.jhtml?articleID=177103404

2. M. Gambhir, V. Dhanasekaran, J. Silva-Martinez, E. Sánchez-Sinencio, "Low power architecture and circuit techniques for high boost wideband Gm-C filters," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 3, pp. 458-468, Mar. 2007.

3. V. Dhanasekaran, M. Gambhir, J. Silva-Martinez, E. Sánchez-Sinencio, "A 1.1GHz 5th order active-LC butterworth type equalizing filter," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2411-2420, Nov. 2007.

4. M. Gambhir, V. Dhanasekaran, J. Silva-Martinez, E. Sánchez-Sinencio, "A low power 1.3GHz dual-path current mode Gm-C filter," in *Proc. IEEE Custom Integrated Circuit Conf.(CICC)*, San Jose, CA, Sep. 2008, pp. 703-706.

5. V. Dhanasekaran, M. Gambhir, M. Elsayad, C. Mishra, L. Chen et al., "A 20MHz BW 68dB DR CT ΔΣ ADC based on a multi-bit time-domain quantizer and feedback element," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper,* San Francisco, CA, Feb. 2009, pp. 174-175.

6. J. Fields, P. Aziz, J. Bailey, F. Barber, J. Barner et al., "A 200Mb/s CMOS EPRML channel with integrated servo demodulator for magnetic hard disks," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper,* San Francisco, CA, Feb. 1997, pp. 314-315.

7. H. Thapar, S. S. Lee, C. Conroy, R. Contreras, A. Yeung et al., "Hard disk drive read channels: Technology and trends," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, San Diego, CA, Sept. 1999, pp. 309–316.

8. P. Pandey, J. Silva-Martinez, X. Liu, "A 500MHz OTA-C 4^{th} order lowpass filter with class AB CMFB in 0.35 μm CMOS technology," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Orlando, FL, Oct. 2004, pp. 57-60.

9. S. Dosho, T. Morie, H. Fujiyama, "A 200-MHz seventh-order equiripple continuous-time filter by design of nonlinearity suppression in 0.25-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 559-565, May 2002.

10. F. Rezzi, I. Bietti, M. Cazzaniga, R. Castello, "A 70-mW seventh-order filter with 7-50 MHz cutoff frequency and programmable boost and group delay equalization," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1987-1999, Dec. 1997.

11. G. Bollati, S. Marchese, M. Demicheli, R. Castello, "An eighth-order CMOS low-pass filter with 30-120 MHz tuning range and programmable boost," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1056-1066, Jul. 2001.

12. I. Mehr, D.R. Welland, "A CMOS continuous-time Gm-C filter for PRML read channel applications at 150 Mb/s and beyond," *IEEE J. Solid-State Circuits*, vol. 32, no. 4, pp. 499-513, Apr. 1997.

13. B. McNeil, "HDD Architectures," (Private Communication), LSI Corp., Allentown, PA.

14. R. Schaumann, M. E. Van Valkenburg, *Design of Analog Filters*. New York, NY: Oxford University Press, 2003.

15. K. Ogata, *Modern Control Engineering,* fourth edition. New York, NY: Prentice Hall, 2001.

16. E.A.M. Klumperink, B. Nauta, "Systematic comparison of HF CMOS transconductors," *IEEE Trans. Circuits Syst. II,* vol. 50, no. 10, pp. 728-741, Oct. 2003

17. W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits Syst. II,* vol. 46, no. 3, pp. 315-325, Mar. 1999

18. J. Silva-Martinez, J. Adut, J.M. Rocha-Perez, M. Robinson, S. Rokhsaz "A 60mW 200MHz continuous-time seventh order linear phase filter with on-chip automatic tuning system," *IEEE J. Solid-State Circuits,* vol. 38, no. 2, pp. 216-225, Feb. 2003.

19. Z.-Y. Chang, D. Macq, D. Haspeslagh, P.M.P. Spruyt, L.A.G. Goffart "A CMOS analog front-end circuit for an FDM based ADSL system," IEEE *J. Solid-State Circuits,* vol. 30, no. 12, pp.1449-1456, Dec. 1999.

20. A. Veeravalli, E. Sánchez-Sinencio, J. Silva-Martinez "A CMOS transconductance amplifier architecture with wide tuning range for very low frequency applications," *IEEE J. Solid-State Circuits,* vol. 37, no.6, pp.776-781, Jun. 2002.

21. S. Pavan, Y.P. Tsividis, "Widely programmable high-frequency continuous time filters in digital CMOS technology," *IEEE J. Solid-State Circuits,* vol. 35, no.4, pp. 503-511, Apr. 2000.

22. L. Luh, J. Choma, J. Draper, "A continuous-time common mode feedback circuit (CMFB) for high impedance current-mode applications," *IEEE Tran. Circuits and Syst. II,* vol. 47, no. 4, pp. 363-369, April 2000.

23. U. Yodprasit and C. Enz, "A 1.5-V 75-dB dynamic range third-order G_m-C filter integrated in a 0.18 μm standard digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1189-1197, Jul. 2003.

24. A. Nedungadi, T.R. Viswanathan, "Design of linear transconductance elements," *IEEE Trans Circuits Syst*., vol. 31, no. 10, pp. 891-894, Oct 1984.

25. B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142-153, Feb. 1992.

26. K. Salimi, E Krummenacher, C. Dehollain, M. Declercq, "Continuous-time CMOS circuits based on multi-tanh linearisation principle," *Electron. Lett*., vol. 38, no. 3, pp. 103-104, Jan 2002.

27. S. Kawahito and Y. Tadokoro, "CMOS class-AB current mirrors for precision current-mode analog-signal-processing," *IEEE Trans. Circuits Syst. II*, vol. 43, no. 12, pp. 843–845, Dec. 1996.

28. G. Efthivoulidis, L. Toth, Y.P. Tsividis, "Noise in Gm-C Filters," *IEEE Trans. Circuits Syst. II*, vol. 45, no. 3, pp. 295-302, Mar. 1998.

29. C. Toumazou, F. Lidgey, and D. Haigh, *Analogue IC Design: The Current-Mode Approach*, Stevenage, U.K.: Peter Peregrinus, 1990.

30. G. W. Roberts and A. S. Sedra, "A general class of current amplifier based biquadratic filter circuits," *IEEE Trans. Circuits Syst. I,* vol. 39, no. 4, pp. 257–263, Apr. 1992.

31. S. S. Lee, R. H. Zele, D. J. Allstot, and G. Liang, "CMOS continuous time current-mode filters for high-frequency applications," *IEEE J. Solid-state Circuits,* vol. 27, no. 3, pp. 323-329, Mar. 1993.

32. J. T. Nabicht, E. Sanchez-Sinencio, and J. Ramirez-Angulo, "A programmable 1.8–18 MHz high-Q fully-differential continuous-time filter with 1.5–2 V power supply," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS),* London, U.K., May 1994, pp. 553–556.

33. S. L. Smith, E. Sanchez-Sinencio, "Low voltage integrators for high-frequency CMOS filters using current mode techniques," *IEEE Trans. Circuits Syst. II*, vol. 43, no. 1, pp. 39–48, Jan. 1996.

34. S. Pavan, T. Laxminidhi, "A 70-500MHz programmable CMOS filter compensated for MOS nonquasistatic effects," in *Proc. IEEE European Solid-State circuits Conf. (ESSCIRC),* Montreaux, Switzerland, Sept. 2006, pp. 328-331.

35. T. Y. Lo and C. C. Hung, "A 1GHz OTA-based low-pass filter with a high-speed automatic tuning scheme," in *IEEE Asian Solid-State Circuits Conf. (ASSCC) Dig. Tech. Papers*, Jeju, Korea, Nov. 2007, pp. 408-411.

36. V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynanen, K. Halonen, "A 1.2V 240MHz CMOS continuous-time low-pass filter for a UWB radio receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 2007, pp. 122-123.

37. J. A. Cherry, W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion: Theory, Practice and Fundamental Performance Limits,* New York, NY: Kluwer, 2002.

38. P. Malla, H. Lakdawala, K. Kornegay, K. Soumyanath, "A 28mW spectrum-sensing reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT DS ADC for 802.11n/WiMAX receivers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 2008, pp. 496-497.

39. G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, et al., "A 14b 20mW 640MHz CMOS CT DS ADC with 20MHz signal bandwidth and 12b ENOB," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, Feb. 2006, pp. 131–140.

40. Y. Tsividis, "Continuous-time digital signal processing," *Electron. Lett.*, vol. 39, no. 21, pp. 551–1552, Oct. 2003.

41. V. Dhanasekaran, "Baseband analog circuits in deep-submicron CMOS technologies targeted for mobile multimedia," Ph.D. Dissertation, Texas A&M University, College Station, TX, Aug. 2008.

42. A. Annema, B. Nauta, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits,* vol. 40, no.1, pp. 132-143, Jan. 2005.

43. R. Schreier, G.C. Temes, *Delta-Sigma Data Converters*, New York, NY: Wiley-IEEE Press, 1996.

44. G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, et al. "A 20-mW 640-MHz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641-2649, Dec. 2006.

45. S. Karthikeyan, S. Mortezapour, A. Tamineedi, and E. K. F. Lee, "Low voltage analog circuit design based on biased inverting opamp configuration," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 3, pp. 176–184, Mar. 2000.

46. L.J.Breems, R. Rutten, R.V. Veldhoven, G.V.D. Weide, H. Termeer, “A 56mW CT quadrature cascaded ΣΔ modulator with 77dB DR in a near zero-IF 20MHz band,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2007, pp. 238-239.

47. M.Z. Straayer, M.H. Perrott, "A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based quantizer and DEM circuit in 0.13um CMOS," in *Proc. IEEE VLSI Circuits Symp*., Kyoto, Japan, Jun. 2007, pp. 246-247.

48. P. Malla, H. Lakdawala, K. Kornegay, K. Soumyanath, “A 28mW spectrum-sensing reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMAX receivers,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2008, pp. 496-497.

VITA

Manisha Gambhir received the B.E. degree in electronics and communication engineering from Delhi University in 2001 and the M.S. and Ph.D. degrees in electrical engineering from Texas A&M University in 2006 and 2009 respectively. She was employed as IC Design Engineer in the Broadband Silicon Design Center, Texas Instruments India from July 2001 to July 2003, where she worked on the design of analog circuits for an ADSL front end. She joined the graduate program in the Department of Electrical Engineering, Texas A&M University in the fall of 2003. She held the position of Engineering Intern with the Wireless Group of Silicon Laboratories (now NXP), Austin during the summer of 2004. She interned with read channel Group of Agere Systems (now LSI), Allentown during the fall of 2005, where she was responsible for design of high speed analog to digital converters for read channel applications. Her research interests include high frequency filters, data converters and design of low-power low-voltage analog circuits. She can be reached through the Department of Electrical Engineering, c/o Dr. Edgar Sanchez-Sinencio, Texas A&M University, College Station, TX 77843-3128.